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Master of Science in Electrical Engineering and Computer Science

Massachusetts Institute of Technology

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Jerome Jeffrey Akerson

Submitted to the Department of Electrical Engineering and Computer Science on May 18, 1990 in partial fulfillment of the requirementsfor the degree of Master of Science in Electrical Engineering and Computer Science.

Abstract

An L-band GaAs dual-gate MESFET monolithic mixer has been developed to convert a 1.575 GHz signal to an intermediate frequency of 173 MHz with a local oscillator frequency of 1.402 GHz. In order to reduce chip size, active baluns and buffer amplifiers have been combined with two dual-gate MESFET mixers to form a single integrated balanced mixer circuit. The active baluns eliminate the need for large passive baluns, and the buffer amplifiers replace the IF matching networks; thus, easing integration at L-band frequencies. Circuit size is 1.15 X 1.8 mm. The circuit was fabricated by TriQuint Semiconductor for the Charles Stark Draper Laboratory; however, this thesis describes only the design, simulation, and layout of the mixer circuit.

Thesis Supervisor: J. A. Kong

Title: Professor of Electrical Engineering

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by

Jerome Jeffrey Akerson

Submitted to the

DEPARTMENT OF ELECTRICAL ENGINEERING AND COMPUTER SCIENCE

in partial fulfillment of the requirements

for the degree of

MASTER OF SCIENCE

in ELECTRICAL ENGINEERING AND COMPUTER SCIENCE

at the

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

June, 1990

Signature of Author _____

Department of Electrical Engineering and Computer Science, May 18,1990

Certified by _____

Qizheng Gu, Visiting Scientist, RLE

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Certified by _____

Peter Nuytkens, CSDL Supervisor

Accepted by _____

Arthur C. Smith, Chair, Department Committee on Graduate Students

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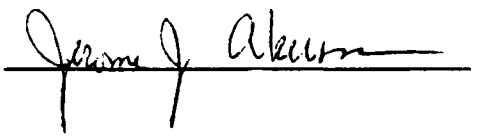

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Finally, I'd be delinquent, if I didn't recognize the one person who kept me sane at work, Frank Mullen. Thanks, Frank.

Dedicated to Dad

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CHAPTER 1

Introduction

1.1 Objective

The objective of this thesis is to investigate monolithic circuit techniques for L-band mixers and compare trade offs between mixer performance and chip size. To achieve the objective, a completely monolithic GaAs dual-gate metal-semiconductor field effect transistor (MESFET) L-band mixer will be developed that converts a 1.575 GHz (RF) signal to an intermediate frequency (IF) of 173 MHz using a Local Oscillator (LO) of 1.402 GHz with the intent that the mixer will be the precursor to a mixer that will eventually become a building block in a totally monolithic receiver system as the first frequency down conversion in a Global Positioning System (GPS) receiver.

The mixer development will be done at the Charles Stark Draper Laboratory in Cambridge, Massachusetts as a secondary goal in an Independent Research and Development (IR&D) project meant to produce a common design environment to design integrated circuits across several semiconductor process technologies. The overall approach is to assemble the necessary CAD tools for selected process technologies and foundries and validate them by designing, building, and testing various circuits. The mixer circuits will fulfill an IR&D sub-goal of MMIC design using a GaAs MESFET technology and the TriQuint Semiconductor foundry in Beaverton, Oregon.

1.2 Background

In order to design a mixer for a monolithic receiver system, it is important to understand the role of the mixer in any receiver system. Figure 1.2.1 represents a receiver that uses two mixers(denoted by circle with cross inside) to convert a received signal to baseband. The first mixer converts the signal to the IF for amplification and filtering and the second mixer converts the IF to baseband. Typically, mixers exhibit conversion loss and a relatively high noise figure, so most receivers contain amplification stages to boost system gain and a Low Noise Amplifier (LNA) to suppress the noise

contributions of the subsequent stages (i.e.mixer) in the system. The band pass filters are used to remove noise power and spurious responses. Improvement in the mixer performance could reduce the number of components necessary for the receiver which would reduce system complexity and size and improve reliability.

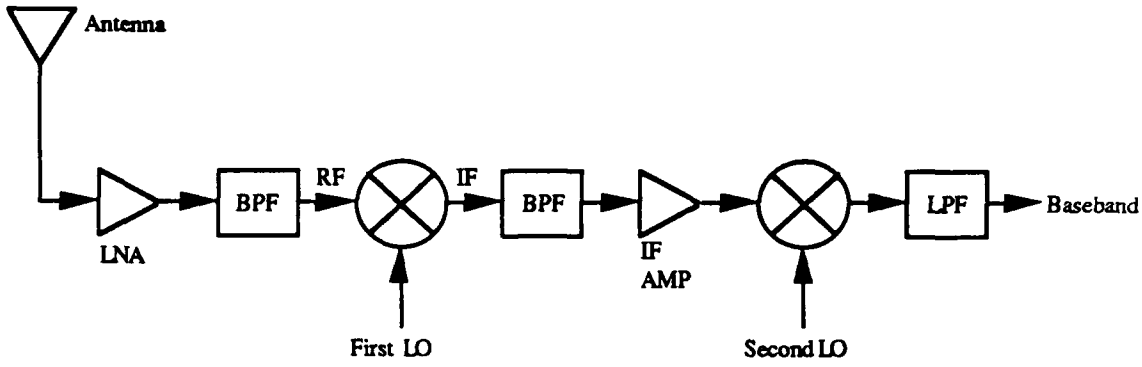

Figure 1.2.1 Receiver system

The schottky diode is the most widely used GaAs mixing device because of its simplicity and well defined nonlinear characteristics. However, a diode mixer typically provides several dB of conversion loss, and all the port-to-port isolation must be provided by space consuming filtering or baluns. Single gate FETs (SGFETs) are becoming popular in mixer designs because of their potential for gain and lower noise figure. For this monolithic mixer, a dual-gate FET is proposed. DGFETs have similar gain and noise characteristics as SGFETs and they offer inherent RF/LO isolation when the two signals are applied to the separate gates of the device. This isolation can greatly reduce the filtering requirements and is ideal for monolithic design.

Although there has been some recent work done in L-band monolithic mixers, the majority of MMIC mixers operate at much higher frequencies. A common monolithic mixer circuit used in direct broadcast satellite (DBS) systems is the single ended dual-gate FET mixer (Figure 1.2.2).

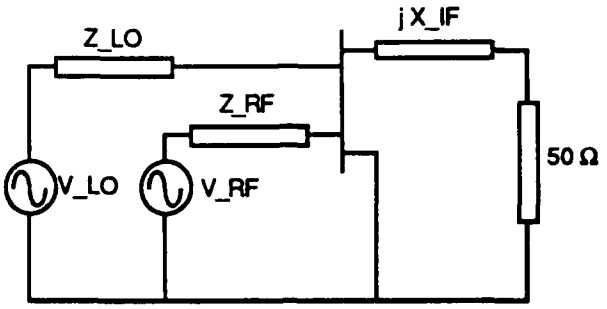

Figure 1.2.2 Single ended DGFET mixer

Kermarrec *et al* [1] used this topology for a DBS system that converted 11.7-12.5 GHz signals to IFs of 0.9-1.7 GHz with a 10.8 GHz LO. For maximum conversion gain, they found that it is desirable to provide an LO and RF short at the output, an IF short at the input, and matching at all three ports. However, even at these relatively high frequencies they found that simultaneous achievement of these goals difficult using monolithic technology. The RF/LO short was implemented with a parallel capacitance at its series resonance and all other matching consisted of spiral inductors and interdigitated capacitors. The chip size was 2.4 X 1.4 mm^2. The circuit provided a maximum conversion gain of 2 dB and a noise figure of 6.5 dB with RF and IF port VSWRs less than 2 and less than 3.5 respectively across the band.

In order to further reduce chip size, Suguira *et al* [2] built a similar circuit but replaced the IF matching network with a buffer amplifier. The mixer and buffer were actually fabricated on two chips measuring 0.96 X 1.26 mm^2 and 0.96 X 0.60 mm^2. Only three impedance conditions were defined as design goals: power match at the RF and LO ports and an LO short at the IF port. The matching consisted of one-section parallel and series microstrip, and a quarter wavelength spiral stub provided the LO short at the mixer output port. Both the DGFET and buffer SGFET were 1 μm long and 320 μm wide. A single stage resistor-capacitor coupled amplifier was used as the buffer amplifier. Together, the mixer and buffer provided 2.9 +/- 0.4 dB of conversion gain with a 12.3 +/- 0.3 dB SSB noise figure across the input band

of 11.7-12.2 GHz. (A 0.9-1.4 GHz IF was obtained with a 10.8 GHz LO.) The RF port VSWR was less than 1.5 while the LO port VSWR was almost 6.

Another monolithic single ended DGFET mixer was developed by Yang *et al* [3] as part of an X-band receiver. On a single chip, they placed a 0.5 X 300 μm DGFET with lumped and distributed matching networks and a low pass filter to suppress the LO and RF signals at the IF port. The RF signal, ranging from 6 to 10 GHz, was converted to a constant 3 GHz IF using a variable LO (9 to 13 GHz). This mixer produced 7 +/- 1.5 dB of conversion loss and provided 20-35 dB of RF/IF isolation and 35-55 dB of LO/IF isolation.

Instead of using a DGFET, Harvey *et al* [4] used a balanced SGFET mixer to down convert 6-4 GHz signals using an LO of 2.45 GHz. As part of a satellite transponder, their mixing "module" consisted of five separate MMIC chips: a signal routing chip, two passive RF/LO combiners, a balanced mixer, and an IF amplifier. The mixer consisted of two 1 μm X 300 μm SGFETs with high impedance microstrip and MIM capacitor matching networks. Balancing was achieved by connecting the drains of the two SGFETs to the same matching network. The mixer chip alone produced 5 dB of conversion loss and a noise figure of 13 dB.

A double balanced DGFET monolithic mixer was presented by Pavio *et al.* [5] Their topology provides a double balance mixer requiring only one balun (Figure 1.2.3) The circuit uses common gate and common source DGFETs as the mixing devices and one balun to provide a balanced RF signal. With this arrangement, the inherent anti-phase relationship between the common gate and common source DGFETs provides anti-phase transconductance swings in the two mixers with a single ended LO signal.

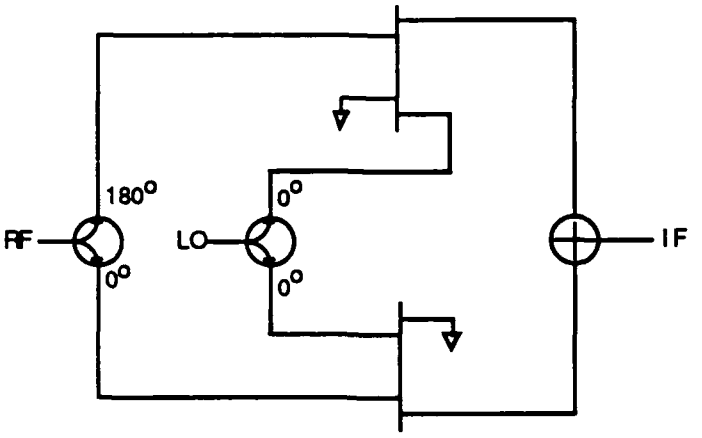

Figure 1.2.3 Common gate/common source DGFET double balance mixer

A distributed monolithic mixer chip using the topology of Figure 1.2.3 along with one active balun chip was built. 0.5 μm X 150 μm DGFETs were used and each chip measured approximately 2 X 2 mm^2. The mixer with balun exhibited approximately 2-3 dB of conversion loss over a very wide band from 3 to 11 GHz. The circuit provided 22-32 dB and 18-30 dB of suppression for the RF and LO respectively at the IF port and greater than 45 dB RF/LO isolation over the entire band.

The only work published on monolithic mixers below 3 GHz is the result of the push to develop a small and inexpensive GPS receiver. The information published by Weber [16] addressing their work on a GPS receiver sheds very little light on the solutions to monolithic design in L-band. Weber explained that to overcome the requirement for large spiral inductors on chip they used active inductors and R-C coupled stages in their design. No performance data was presented. On the other hand, the work presented by Benton *et al* [6] provided more specifics. On a single chip, 1.2 X 1.2 mm^2, they provided RF and IF amplification, an LO buffer and a double balanced mixer. The RF amplifiers provide gain, reduce subsystem noise, and decrease the LO and IF leakage out of the RF port. The LO amplifier buffers reduce the LO power requirements. Finally, the IF amplifiers provide gain, increase the power output, and reduce the spurious response by adding power at the IF. The mixer chip provided 20-25 dB of conversion gain.

There are several reasons why a direct quantitative comparison between the previous mixers is difficult. First, each group of authors presented a different set of results. The only parameter in common is conversion gain. Also, each mixer design weighted performance parameters differently. Finally, since the mixers were part of larger systems, the relatively poor performance of a mixer, such as conversion gain and interport isolation, was more than likely compensated by another portion of the system. The distributed and lumped element matching at all three ports would be difficult at L-band; but, DGFET topologies, balanced approaches, and the use of buffer amplifiers offer the most promise in an L-band design.

1.3 Overview

Although the mixer topology being developed is intended for general L-band applications, the frequency specifications and design goals of the mixer circuit are based on the Global Positioning System (GPS) requirements. GPS was selected because of the great interest in completely integrating a GPS receiver. In the earlier years of GPS, Draper developed a down mixer for a GPS receiver that was assembled in a box that measured 8" by 4" by 2.5". The design goals for the monolithic mixer were derived, although greatly simplified, from these original mixer specifications.

Several DGFET mixer topologies and balun types were investigated. The circuits were divided into logical subcircuits and laid out separately on the wafer to better understand dual-gate FET mixer operation. Keeping a monolithic receiver in mind, the emphasis was to optimize the performance of the mixer in order to reduce the performance requirements of other on-chip receiver components such as filtering and gain stages. For example, if LO/IF isolation of the mixer can be improved 10 dB by a better mixer design, then the suppression requirements of subsequent filtering stages may be relaxed by 10 dB possibly allowing the removal of an entire filter stage.

The circuits were designed for fabrication on a 4" wafer using TriQuint's QED/A 1 μm GaAs MESFET process. The process is capable of producing depletion and enhancement FETs, DGFETs, schottky diodes, implanted resistors, thin film resistors, airbridge inductors, MIM capacitors, and vias.

The final circuit designs were simulated using commercially available non-linear and linear circuit analysis software programs. The non-linear

programs include Microsim's PSpice and EEsof's Libra. Libra uses a harmonic balance technique and PSpice uses strictly time domain analysis. To perform linear circuit analysis, EEsof's Touchstone was used. The non-linear tools were used to predict bias points, conversion gain, spurious response, and isolation, whereas the linear tool was used to aide matching and predict VSWRs. All non-linear and linear device model parameters and process parameters were obtained and/or derived using the foundry's published specifications. The predicted conversion gain, spurious response, isolation, and input/output VSWR of the mixer and the predicted gain and phase and amplitude balance of the baluns are presented.

The circuits were designed so that all testing may be done on the wafer using a Cascade Microtech wafer probe station. This eliminates test fixtures and packaging requirements. Various 6 mil pitch probing points were incorporated into the layout for the application of bias and RF and LO signals and the extraction of the IF. Furthermore, DC test points were laid out to better understand the circuit operation.

The circuit layout was done using GDT. A TriQuint QED/A process specific "technology file" was developed, so that GDT can produce the CALMA/GDS II files necessary to fabricate each of the 15 masks. The "technology file" contains process design rules such as the transistor layers and dimensions, minimum spacing between layers, and process parameters such as inter-layer capacitances, material resistivity etc. This information enables GDT to verify that design rules are met and to extract layout parasitics.

These circuits returned from TriQuint will be the very first Draper circuits built by TriQuint Semiconductor. Therefore, they are the first circuits built using the modified CAD tools. The performance of these circuits will validate Draper's design tools, point out discrepancies, and validate the feasibility of a DGFET as an L-band mixing device. This thesis, however, only documents the development of the L-band monolithic mixer from design through start of fabrication. The actual circuit measurements will be published in the Draper IR & D Project 238 Annual Report. In the following thesis chapters, Chapter 2 briefly describes the mixing process, the mixer design goals, the challenges of L-band monolithic design followed by a qualitative analysis of DGFET mixer topologies against those goals. With a topology selected, Chapter 3 contains detailed modeling and simulation of the DGFET devices, DGFET circuits, and balun circuits Chapter 4 describes the

fabrication and layout process and final "as-built" circuits and a discussion of the layout parasitics. Chapter 5 presents a discussion of the problem areas of the design and recommendations for alternate approaches for monolithic L-band mixer design to be incorporated into the next wafer run. Chapter 6 summarizes and reports the conclusions.

CHAPTER 2

Analysis

2.0 Ideal Mixer

An ideal mixer can be thought of as a perfect multiplier with two input ports for the RF and LO signals and one output port for the IF. Figure 2.0.1 represents an ideal mixer that multiplies two cosine waveforms at two different frequencies, f_{RF} and f_{LO}, and produces at the IF port the sum and difference frequencies, $f_{RF}+f_{LO}$ and $f_{RF}-f_{LO}$. For down conversion, the sum frequency would be removed with a low pass filter (LPF) preserving the difference frequency. Similarly, during up conversion the sum frequency is saved while removing the difference with a high pass filter (HPF).

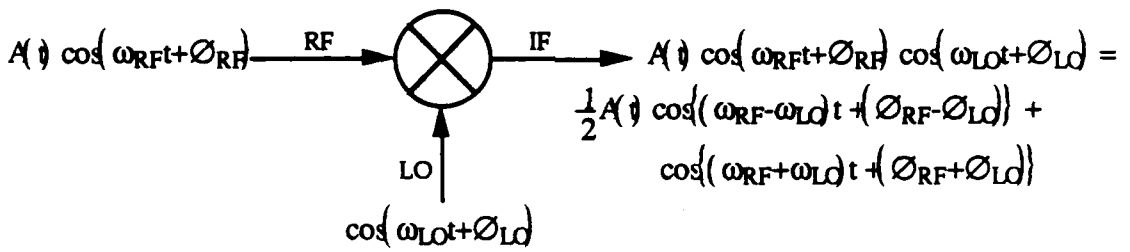

Figure 2.0.1 Ideal multiplier as a mixer

A real mixer is never a perfect multiplier. Usually any non-linear device can be used as a mixer. For example, the I-V characteristics of a non-linear device can be represented by a series expansion: $I=a_0+a_1V+a_2V^2+a_3V^3+a_4V^4+....$ If the voltage ,V, is the sum of the RF and LO waveforms, the resulting current will contain all the harmonics of the RF and LO and their intermodulation products. Also, if the coefficient a_1 was proportional to the RF signal and V was proportional to the LO (and visa versa) signal mixing would occur.

Quantitatively, the frequencies at the output will be $mf_{RF}+nf_{LO}$ and the corresponding phases will be $m\phi_{RF}+n\phi_{LO}$ where $m=0,\pm1,\pm2,\pm3,...$ and $n=0,\pm1,\pm2,\pm3....$ A given frequency is often conveniently represented by

(m,n). For example, the desired downconverted IF would usually correspond to m=+1 and n=-1 or (1,-1). The LO and RF harmonics would be represented by (0,n) and (m,0) respectively for all n and m not equal to zero. Finally, when $|m|=1,2,3,...$ and $|n|=2,3,4,...$ or $|m|=2,3,4,..$, and $|n|=1,2,3....$, the output frequencies are called intermodulation products. In general, only the IF is desired and the other products become the unwanted spurious response and must be removed with filtering and/or a balanced mixer design.

2.1 Mixer Design Goals

The specifications of the original mixer designed and built at Draper Lab contained the following design goals. The mixer must convert the received signal of 1575.41 MHz (RF) to 173.91 MHz (IF) using an LO of 1401.51 MHz. The signal bandwidth is 20.46 MHz with prime consideration given to the gain stability, phase linearity, and spurious rejection. The Voltage Standing Wave Ratio (VSWR) should be a maximum of 2.0 for the RF port and a maximum of 1.5 for the IF and LO ports as seen by a 50 Ω system. The transfer characteristics include a conversion gain of 32 dB, a SSB noise figure of 21 dB at the IF, and a deviation from linear phase of +/- 16° at the IF +/- 6 MHz. Finally, the LO/RF and LO/IF isolation should be 30 dB minimum, and the spurious response of order >2 and <7 should be less than 50 dB compared to the IF. [7] It is not the intent of this thesis to design a mixer chip that meets all the above specifications, instead the specifications will be used as guidelines which will help weight performance criteria and, thus, influence the design.

Since providing isolation, spurious rejection, and impedance matching require the largest portions of the chip, the design goal will be to optimize the trade off between chip size and performance in those areas. The matching will be done to 50 Ω since the mixer will be tested and simulated in a 50 Ω environment and, more importantly, it will allow easier comparison to other mixers. Although gain is desired, it will take a secondary role in the optimization because gain stages do not usually require a lot of space. Noise figure, although very important in a receiver system, will also be given secondary consideration for several reasons. First of all, an LNA will be used in the receiver. LNA design techniques are very well defined and easier to implement with a two port device. Secondly, DGFET noise models have not been developed and will not be considered in this thesis. Thirdly, a low drain

current operating point will be selected, and a relatively "low noise" operation will be expected.[8]

2.3 Physical Limitations

As previously mentioned, monolithic design in L-band poses certain challenges. The fundamental problem is that the low frequency translates directly into large matching and filtering elements and balun sizes. The wavelength, λ, in a length of microstrip is given by equation 2.3.1 where λ_o

$$\lambda = \lambda_o/(e_{ff})^{1/2} \qquad (2.3.1)$$

is the free space wavelength and e_{ff} is the effective relative dielectric constant of the microstrip. The effective relative dielectric constant is a function of the relative dielectric constant and the physical dimensions of the microstrip and its height above the ground plane.[9] At 1.575 GHz a 50 Ω quarterwave line is over 16 mm long which is obviously too large to be used in a monolithic design. Similarly, the size of the reactive components in a L-band circuit can be overwhelming. Recall that capacitance, C, and inductance, L, for a given frequency, f, and impedance magnitude, Z, are given by equations 2.3.2 and 2.3.3.

$$C = 1/2\pi fZ \qquad (2.3.2)$$

$$L=Z/2\pi f \qquad (2.3.3)$$

Thus, for a given impedance, as the frequency decreases the capacitor and inductor sizes increase. For example, looking into the gate of a typical 300 μm wide FET at 1.575 GHz the reactance is approximately -150 Ω. For a conjugate match, a 15 nH series inductor would be required taking up over $(400\ \mu m)^2$ of chip space. Similarly, microwave circuits usually rely on rf coupling/DC blocking capacitors to isolate subcircuits. These capacitors ease integration of subcircuits into a system at the expense of chip area. Even a capacitor as small as 2.5 pF is still large at 95 μm^2 and provides an impedance of 40 Ω and 360 Ω at 1.575 GHz and 173 MHz. With sizes this big very few components would fit on the chip. Thus, when selecting a mixer topology, it will be desirable to minimize the number of passive reactive components.

2.4 Circuit Topologies

To this end, a balanced DGFET mixer is proposed. Diode and single gate FET mixers were immediately discounted because of the space consuming filtering required to provide the RF/LO isolation. If lumped

element filters were used to provide the necessary 30 dB of RF/LO isolation, since the RF and LO frequencies are close, 9 or 10 reactive elements would be needed. [21] Similarly, single ended DGFET mixers were discounted because of the filtering required to provide the LO/IF isolation and spurious rejection. A balanced DGFET mixer offers a high degree of isolation and spurious rejection without any filtering. If active baluns are used, the added mixer and baluns still lead to a much smaller design. The design of any balanced mixer can be divided into three major parts: the mixer, the baluns, and the matching networks.

2.4.1 Balanced Mixer Topologies

There are essentially two types of balance DGFET mixers: single balanced (SB) and double balanced (DB). A single balanced DGFET mixer uses a balun to split the LO or RF signal and introduce a 180° phase difference between the two outputs. These outputs are then fed into two separate single ended DGFET mixers, and the two IF signals are recombined to form the overall mixer output. Figure 2.4.1.1(a) represents a single-balanced mixer using a balun to provide a balanced LO signal. Consider the frequency products (m,n) and their phases at the output of each mixer. Since the two mixers are identical, both outputs will experience equal phase shifts due to the propagation through the mixers. However, the phase shift at the output due to the phase of the RF and LO signals will be $m\phi_{RF}+n\phi_{LO}$ for the mixing product (m,n). In the case of a SB mixer, the output phase of the upper mixer will be 0° and the output phase of the lower mixer will be n(180°). Therefore, all products, (m,n), with n odd will be out of phase with respect to each other and all products with n even will be in phase. So, if the two output signals are subtracted as shown, the IF will be preserved while the even LO responses will be rejected without filtering.

A double balanced approach uses two baluns and feeds two single ended DGFET mixers (Figure 2.4.1.1 b). The 0° LO and 180° RF signals are fed into one of the mixers while the 180° LO and the 0° RF signals are fed into the other. Similar analysis to that use for the single balanced mixer shows that the output phase of the upper mixer will be m(180°) and the output phase of the lower mixer will be n(180°). Now if the two outputs are added (simply by connecting the two drains to the same matching network[4]), the IF signals will add since they are in phase and the odd harmonics of the LO and RF will

cancel since they are 180° out of phase. Furthermore, any LO noise will also cancel at the output. Essentially, each DGFET acts as a short circuit to each other for the odd harmonics of the LO and RF signals without filtering.

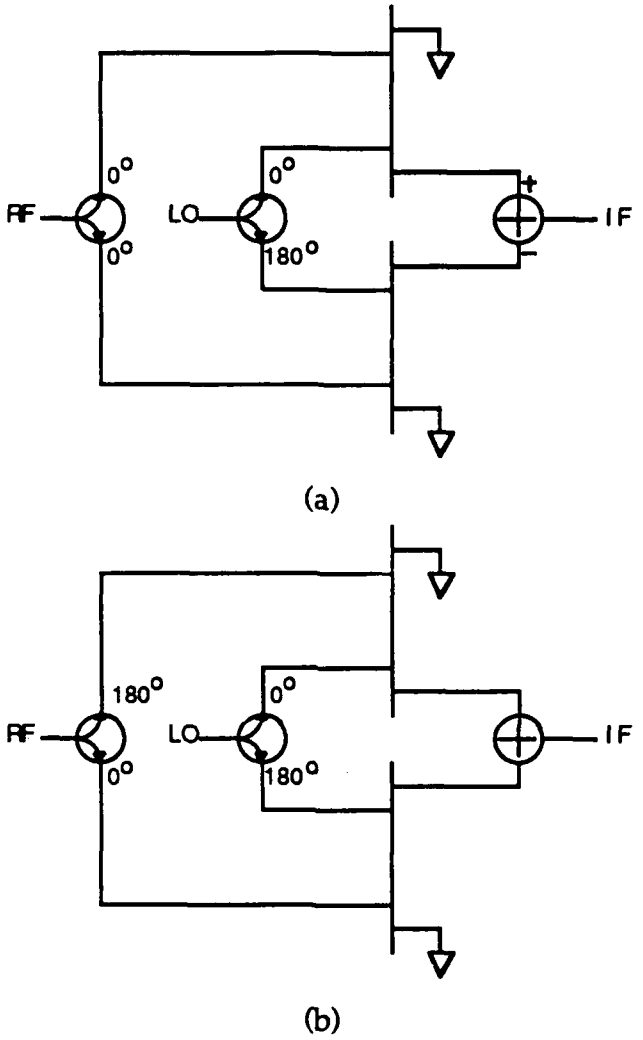

Figure 2.4.1.1 Single balanced mixer (a) Double balanced mixer (b)

Another double balanced approach (double double balanced), presented by Maas [10], rejects both the odd and even harmonics of the LO and RF signals. (Figure 2.4.1.2) Here each DGFET pair rejects LO noise and the odd harmonics and the final subtraction rejects the even harmonics while retaining the IF signal.

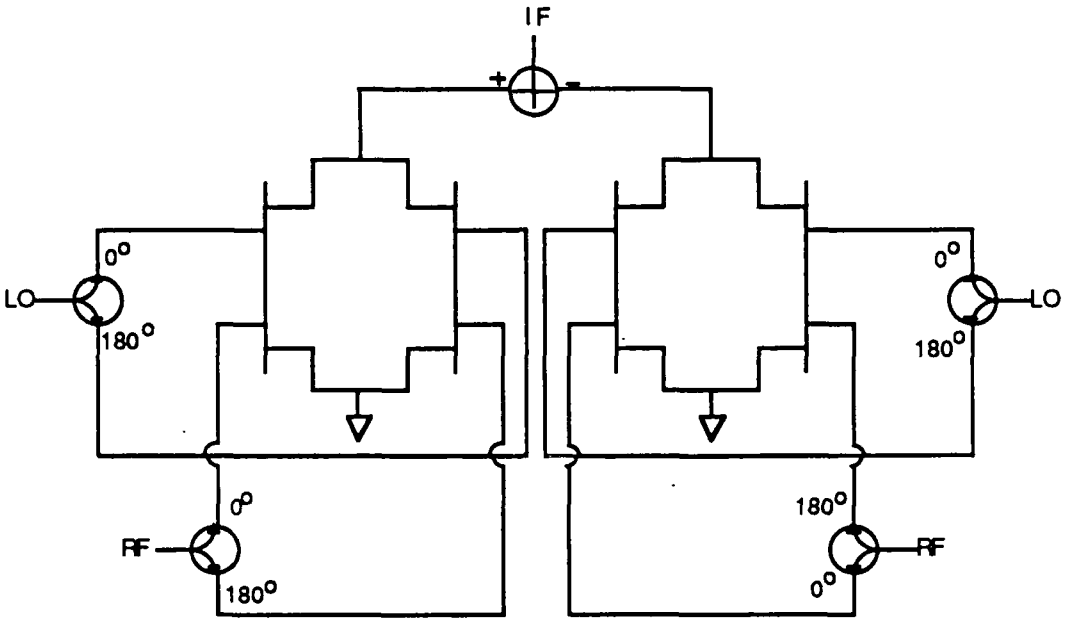

Figure 2.4.1.2 Double double balanced mixer using four DGFETs

It is important to realize that the ability of any balanced mixer to reject LO noise and spurious responses depends on the amplitude and phase balance of the mixer and baluns. For integrated circuits, balance should be very good; however, care must be taken to lay out a circuit that is fairly insensitive to process variations. Furthermore, as more devices are used the more LO power and chip space will be required.

Since a high level of LO/IF isolation is desired, it is important to suppress the LO component (0,1). However, as discussed, providing an LO short and IF match is difficult. A mixer topology that supresses the odd harmonics is desirable. Both the SB and DB mixer topologies suppress the odd harmonics, but the SB topology requires three subcircuits, input balun, mixer, and output balun, whereas the DB topology only requires only two, the input balun and the mixer. The DB mixer topology offers the same spurious suppression but is attractively less complex. The DDB mixer topology offers the best suppression (both odd and even spurs) but is twice as big, requires twice the power, and is more complex. The closest even harmonic is the second LO harmonic (0,2) at 2.8 GHz and can easily be filtered from the IF on chip. The advantage of this type of mixer would be the suppression of the

(2,2) spur at 346 MHz but at a very high cost. For these reasons, a double balanced mixer topology was selected. This type of topology will hopefully provide the majority of the isolation and spurious rejection while the baluns and/or buffer amplifiers as shown by Suguira [2] and Benton [6] will provide the majority of the gain.

2.4.2 Balun Topologies

With a balanced design, the balun becomes an integral part of the overall mixer. Since conventional passive baluns such as Lange couplers are too large for a monolithic design, active baluns are used exclusively in the design. Since the DB mixer topology was selected, only one type of balun will be required: one that takes a single ended signal to balanced signal.

To convert single ended signals to balanced two different baluns offer the most potential. The first balun uses the inherent 180° phase shift between common gate and common source FETs (Figure 2.4.2.1(a)). [5] When a voltage is applied to the input node the drain currents in the upper and lower FETs are 180° apart. This topology is small and simple but is very sensitive to bias and process variations. The second balun, which is less sensitive to process variations, is the well known differential pair (Figure 2.4.2.2(b)). The lower two FETs act as a current source. As Vin swings between its maximum and minimum values the current distribution changes between the upper left and right FETs. As Vin ramps upward the drain current of the upper left FET increases at the expense of the drain current of the upper right FET. Thus, the output node voltages are 180° out of phase.

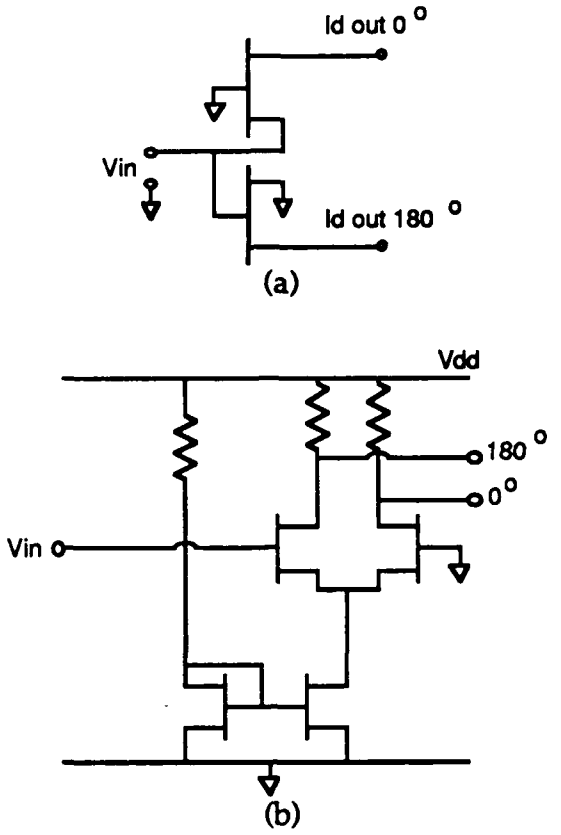

Figure 2.4.2.1 Active input baluns (a) common gate/common source FETs (b) differential pair

The differential pair was selected as the balun topology for this mixer. Although somewhat bigger, the differential pair balun offers better amplitude balance compared to the common gate/common source configuration because changes in Vin not only affect Vgs of the lower FET but also Vds since the drain conductance is not ideally zero. These Vds changes do not occur for the top FET and, thus, create an amplitude imbalance which is strongly dependant on bias conditions.

2.4.3 Matching Networks

Providing matching at all three ports of the mixer is always desirable. A match at the LO, RF, and IF frequencies at the respective mixer ports provides maximum power transfer at the desired frequency and can provide rejection of other frequencies. However, as discussed, at L-band frequencies, there is a trade off in circuit size and performance of the match.

The Smith chart is a useful tool to describe and design matching networks. Recall that the center of the Smith chart represents a normalized impedance of 1 or, in this case, 50 Ω/50 Ω. The left most point represents a perfect short (an impedance of zero or infinite admittance), and the right most point represents a perfect open (infinite impedance or zero admittance). The horizontal axis represents purely resistive impedance or conductive admittance. Above and below the axis represent impedances with positve and negative reactance respectively. The circles completely within the Smith chart represent constant resistance or conductance, and the curves subtended by the Smith chart represent constant reactance or susceptance depending on which set of curves. To develop a matching network with the Smith chart the impedance at the desired frequency (or equivalently the reflection coefficient S_{11}) must be measured and entered onto the Smith chart. For example, S_{11} of gate 1 of a 300 μm depletion TriQuint DGFET at 1.575 GHz is predicted to have a magnitude of .965 and an angle of -29° which corresponds to an impedance of 13.8 -j190 Ω as shown by point A on Figure 2.4.3.1. To match to 50 Ω , starting at the load impedance the designer traverses along constant resistance or conductance circles until reaching the center. By measuring the changes in reactance or susceptance the size of the inductor or capacitor can be calculated. The problem with matching at low frequencies to a capacitative load is evident by the location of point A on the Smith chart. S_{11} is located on the area of the Smith chart where small movements along constant resistance circles represent big changes in the normalized reactance/susceptance. To realize the matching network in Figure 2.4.3.1 two series inductors and one shunt inductor are required. (Figure 2.4.3.2)

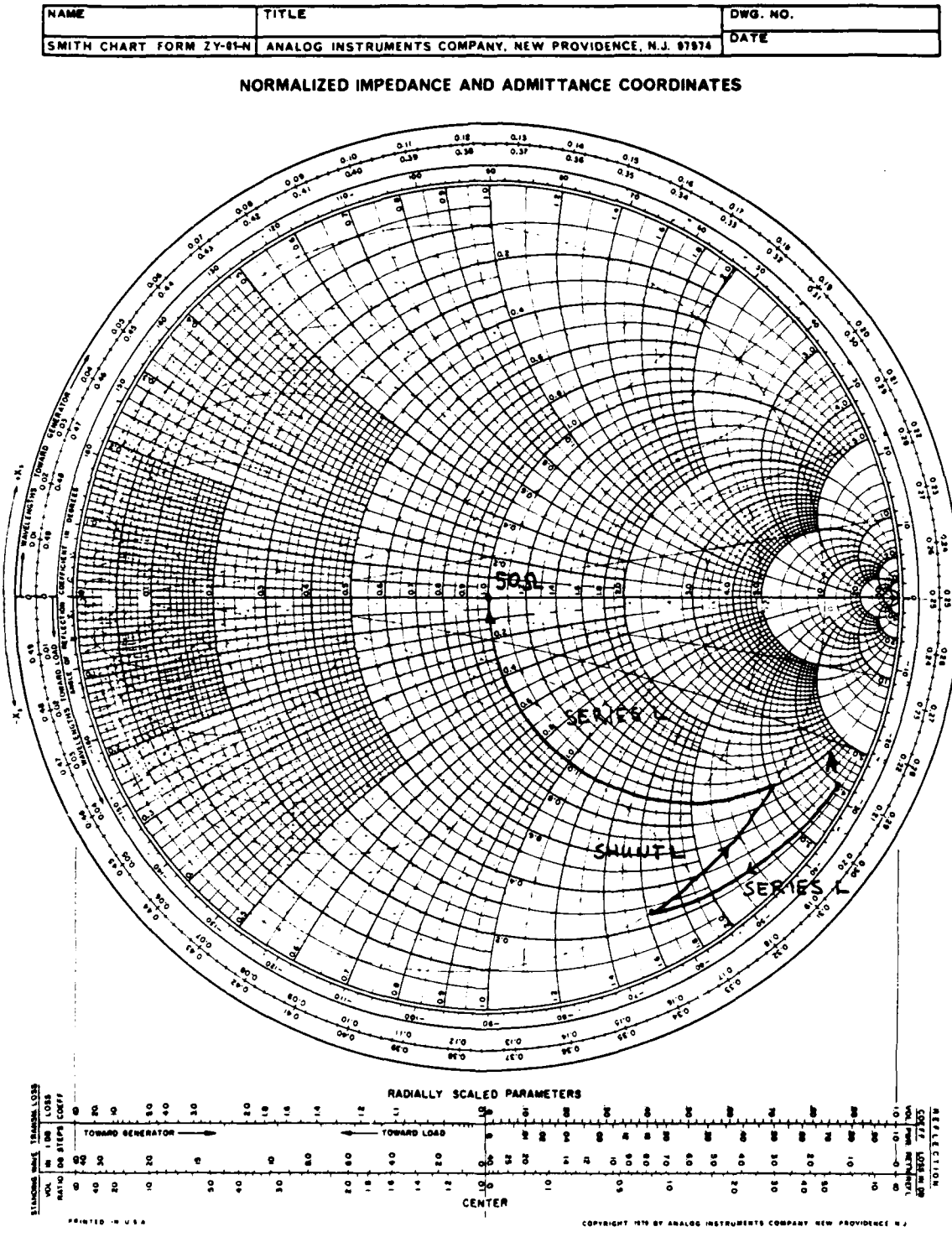

Figure 2.4.3.1 Smith chart with design of matching network.

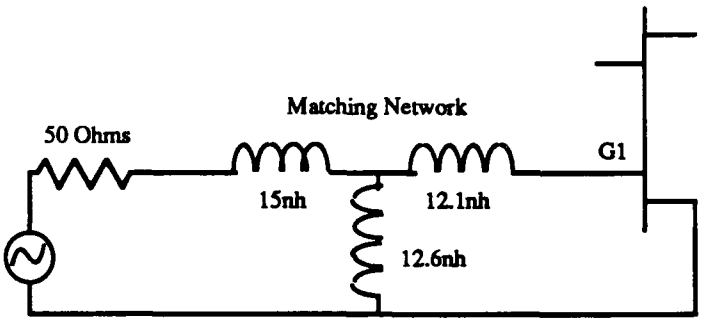

Figure 2.4.3.2 Realization of matching network from Figure 2.4.3.1

It is possible to produce inductors of this magnitude on chip; however, as mentioned earlier they would require a major portion of the chip area. Other paths may be taken on the Smith chart to provide a match, but they all require a lot of space.

For the first pass of the mixer design, this type of matching will not be attempted and the design will concentrate on the circuit topology. The result will be the loss of some gain and frequency selectivity at the input. However, to prevent reflections at the probe tips, resistive matching will be used to improve the VSWR.

CHAPTER 3

Modeling and Simulation

The objective of this chapter is to document the device models and circuit simulations used to develop the L-band mixer. Since this was the first time Draper Lab used the TriQuint Semiconductor GaAs foundry, TriQuint's device models were incorporated into Draper's existing circuit simulation programs. TriQuint has extensively characterized their QED/A single-gate MESFET devices, and therefore, the SGFET models used were taken directly from TriQuint literature. On the other hand, they have not characterized the QED/A DGFET; thus, time is spent developing and understanding the DGFET model used for this mixer before any circuit simulations occur.

3.0 TriQuint MESFETs

The TriQuint QED/A process is capable of producing both enhancement- and depletion-mode 1 μm MESFETs. Three different FETs are available: E-FETs, D-FETs, and M-FETs. The a typical 50 μm wide E-FET (enhancement-mode FET) has a threshold voltage of +.15 V, a maximum drain current of 3 mA (Vds=1.6 V, Vgs=0.7 V), and a transconductance of 5.0 mS (Vds=1.6 V, Vgs=0.5 V). A typical 50 μm wide D-FET (depletion-mode FET) has a pinch-off voltage of -0.6 V, a saturation current of 2 mA (Vds=1.6 V, Vgs=0.0 V), and a transconductance of 5.5 mS (Vds=1.6 V, Vgs=0.0 V). The third FET, called an M-FET or "mixed"-mode FET, is constructed using a channel with both depletion an enhancement layers which provides a larger current capable depletion-mode FET. A typical 50 μm wide M-FET has a pinch-off voltage of -2.0 V, a saturation current of 12 mA (Vds=1.6 V, Vgs=0.0 V), and a transconductance of 9.16 mS (Vds=1.6 V, Vgs=0.0 V). Table 3.0.1 summarizes the TriQuint FET data.

Parameter	E-FET	D-FET	M-FET*
Pinch off Voltage (V)	0	-0.6	-2.0
Current (mA)	3	2.0	12
Transconductance (mS)	5	5.5	9.2

*scaled from a 300 um wide M-FET

Table 3.0.1 Table of typical QED/A 50 μm FET parameters.[20]

3.1 SGFET model

TriQuint provides two models: a nonlinear SPICE model used in SPICE based circuit simulators and a small signal model used in linear circuit simulators.

3.1.0 SGFET SPICE Model

The most widely used SPICE models were developed by Walter Curtice [23] (the Curtice model) and H. Statz *et al* (the Raytheon-Statz model) [11] TriQuint found that these SPICE models do not accurately predict drain conductance over a very wide range of biases. As the device current increases, the models predict drain conductances too large, and for small drain currents the drain conductances are too low. (Figure 3.1.0.1) If these SPICE models are linearized to perform AC analysis these discrepancies create the largest errors in S_{22} and S_{21}. Therefore, TriQuint made slight adjustments to the device equations in order to better predict the drain conductance.

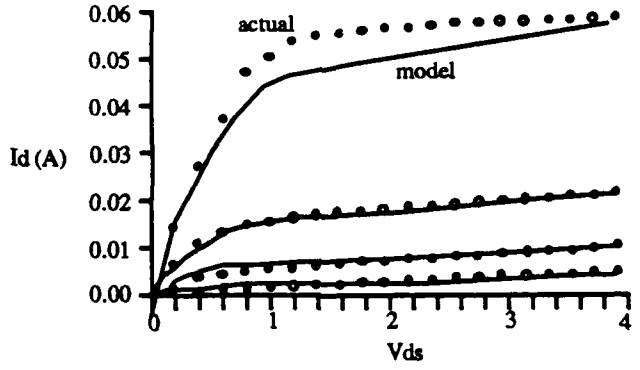

Figure 3.1.0.1 TriQuint FET I-V curves: actual versus Raytheon-Statz model'

TriQuint started with a Raytheon-Statz model [11] and modified it in essentially two ways. First, to improve the drain conductance for low drain currents, a Vds dependence is added to the pinch-off voltage. (Eq. 3.1.1)

$$Vt = Vto + \gamma Vds \qquad (3.1.1)$$

This Vds dependance causes the knee of the I-V curves to shift left to a lower Vds value, therefore increasing the drain conductance. The second change attempts to model the flattening of the I-V curves due to device self-heating. Typically, as the device power increases and the device heats up, the current decreases. With a new parameter, δ, (a function of device power dissipation and thermal impedance) this feedback is modeled by equation 3.1.2.

$$Ids = Idso/(1 + \delta Vds * Idso) \qquad (3.1.2)$$

Idso is the original Raytheon-Statz current modified with the Vds pinch-off voltage. The circuit parameters were derived by fitting the device equations and circuit elements of the model (Figure 3.1.0.1) to the actual device measurements. (The device equations characterize the drain and diode currents and Cgd and Cgs of Figure 3.1.0.3) With the TriQuint model, the I-V curves fit very well for all drain currents and the S-parameters fit over a much larger range of biases over the Raytheon-Statz model.[20]

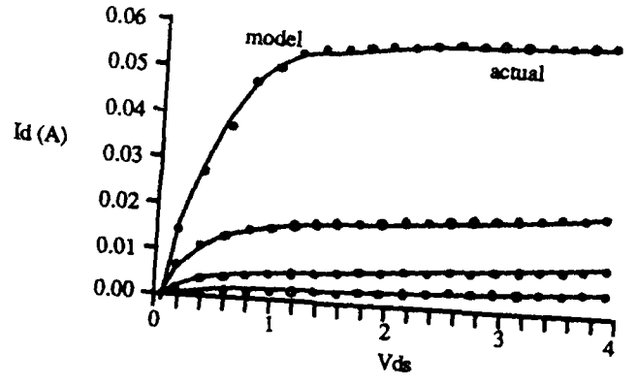

Figure 3.1.0.2 TriQuint FET I-V curves: actual versus TriQuint modified Raytheon-Statz model'

With the circuit parameters normalized to unit area (gate width*gate length =1), the SPICE program scales them according to the area of the FET. The resistances, R_D and R_S, are inversely proportional to the area while R_G is a constant 1 Ω, and the capacitances, CDS, Cgs, and Cgd, and the drain current are directly proportional to the area. [12]

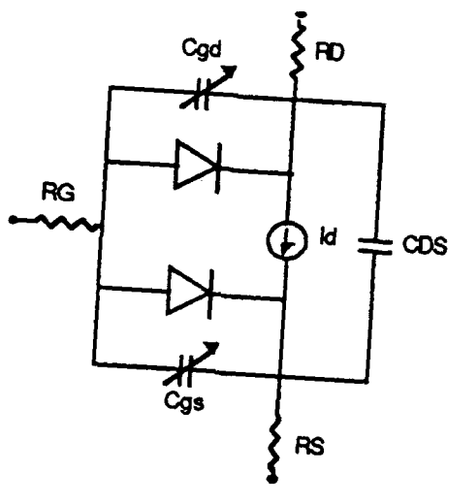

Figure 3.1.0.3 SPICE GaAs FET model

3.1.1 SGFET Linear Model

Since SPICE programs are not well suited for impedance and VSWR measurements, therefore it was necessary to linearize the devices and use a linear simulator. There are two methods for obtaining a linear model: first, take the SPICE model and linearize it at a set bias or, second, fit small signal measurements to a linear model. TriQuint's linear circuit model was developed by fitting the model of Figure 3.1.1.1 to actual S-parameter measurements. The parameter values are functions of bias and can be scaled as in the SPICE model. Let W is the width of each gate finger and N the number of gate fingers (gate length is always 1 μm), then Rds, Rs, and Rd are inversely proportional to the area (W*N) (Rin is a constant 100k Ω); Cds, Cgs, Cgd, and gm are directly proportional to the area; and Lg, Ld, and Ls are proportional to W/N. [13]

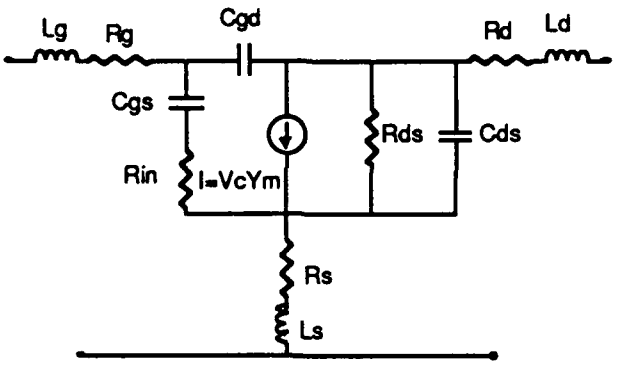

Figure 3.1.1.1. Linear FET model

3.2 DGFET model

Maas [10] points out that one of the problems with using a DGFET is the complexity of the equivalent circuit. An accurate model of the DGFET has not been developed; however, for practical applications, knowledge of a process's SGFETs can produce a useful DGFET model. Since TriQuint does not provide a DGFET model or data for their QED/A process, the DGFET model was derived from their SGFET data.

Tsironis's *et al* [8,14] work showed that a DGFET can be modeled as two SGFETs in series. (Figure 3.2.1)

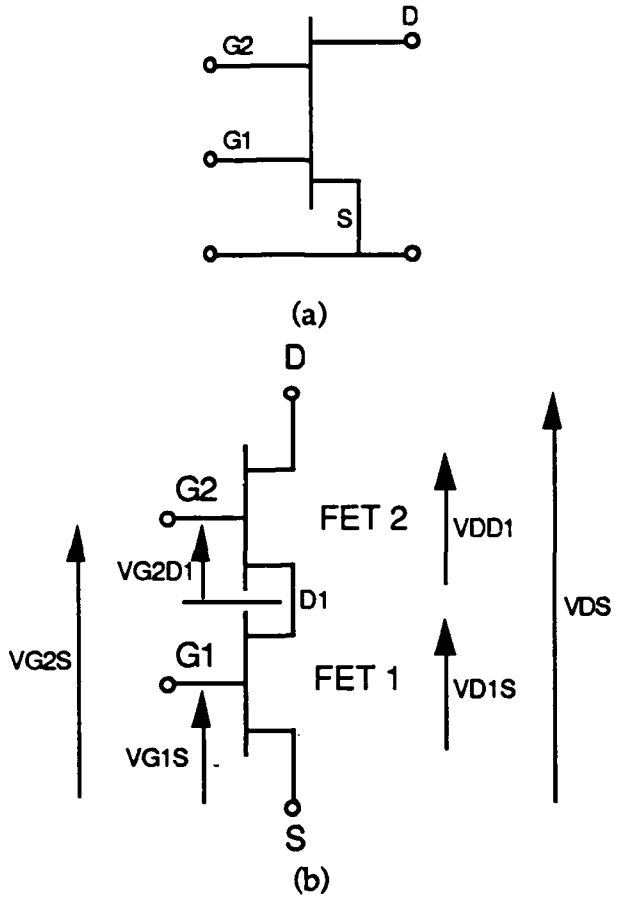

Figure 3.2.1 DGFET modeled as two SGFETs (a) the DGFET and (b) the SGFET model

3.2.0 DGFET SPICE Model

When modeling a DGFET for SPICE programs this way, it is important to understand the differences between the model and an actual device. The first major difference is that the internal channel resistance between the gates is modeled as the the source resistance of FET 2 in series with the drain resistance of FET 1. Large errors in the predicted resistance will alter the I-V characteristics of the device. TriQuint recommends reducing the intergate resistance by half as rule of thumb; however, for large devices the drain and source resistances are so small that this discrepancy can be ignored. This reason helped influence the selection of a large DGFET (300μm wide). Secondly, the drain-to-source capacitance, Cds, is underestimated because it is modeled as two Cds's in series. The actual DGFET Cds should be comparable

to that of a SGFET because it is a geometry driven effect and the actual geometries are very similar. At L-band frequencies, non-linear simulations using both the larger and smaller Cds values have little noticeable effect and was ignored during the mixer simulations.

3.2.1 DGFET Linear Model

The DGFET linear model used was also two single gate FETs connected together. (Figure 3.2.1.1) Where the two FETs models come together the inductances were removed and the source and drain resistances were replaced by R_{12}. (TriQuint recommends $R_{12} = R_D$) Furthermore, the drain to source capacitances are reduced to zero and replaced with a single Cds. Unlike the SPICE simulations, when using the linear model, the discrepancies were not ignored because of the effect they have on the output impedance.

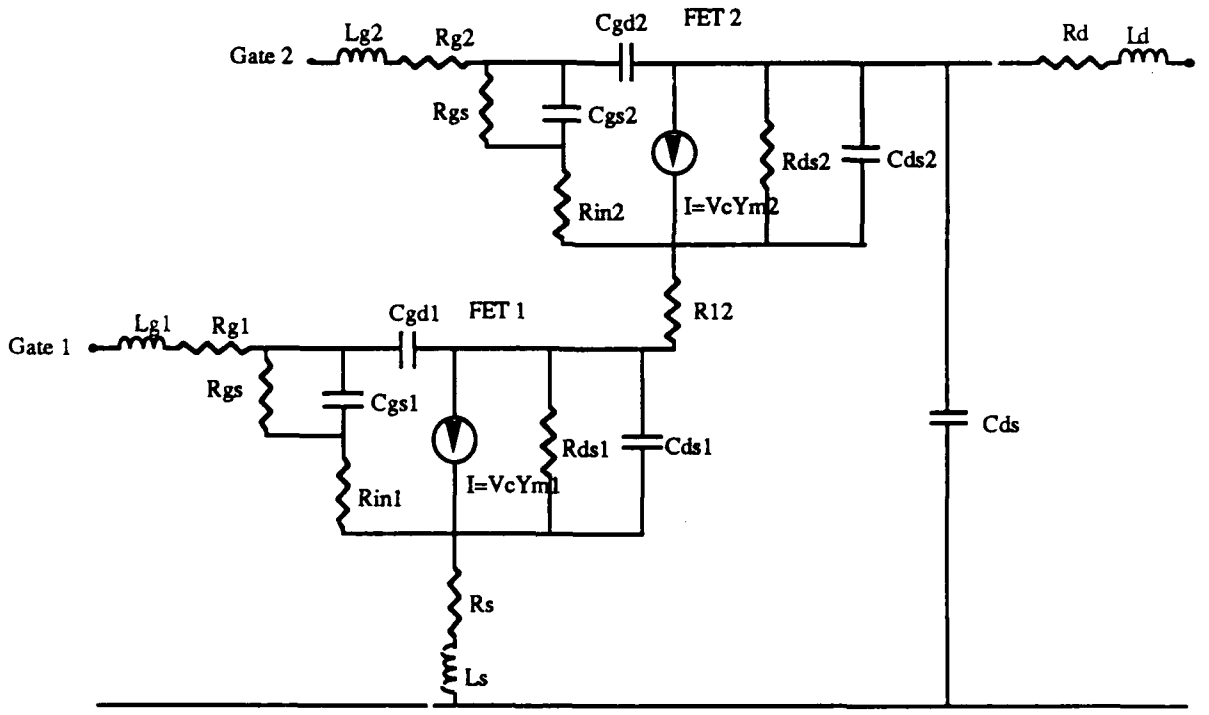

Figure 3.2.1.1 DGFET linear model.

The element values were obtained by determining the operating point of each SGFET using SPICE and reading the element values from TriQuint published tables. Figure 3.2.1.2 represent the S-parameters from 300 kHz to

3GHz looking into gate 1 (S_{11}), gate 2 (S_{22}) and the drain (S_{33}) of a 300μm D-type DGFET with V_{DS}=3V and V_{G1S}=V_{G2S}=0V. The frequencies of interest are marked for the respective ports.

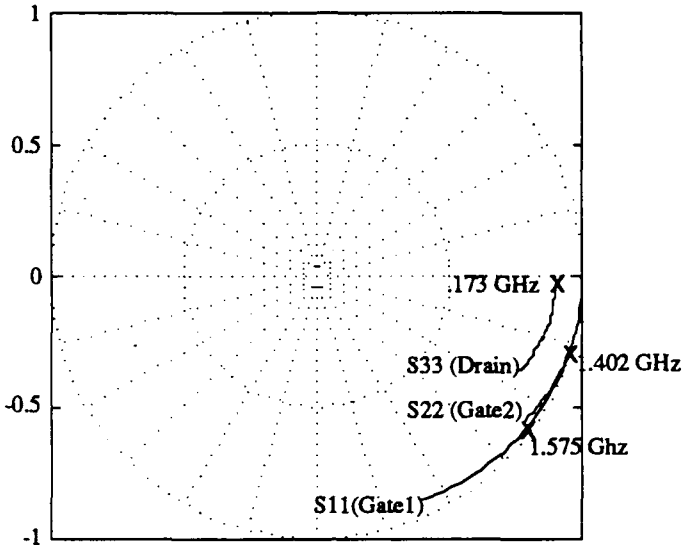

Figure 3.2.1.2 S-parameters of 300μm D-type DGFET 300 kHz to 3 GHz

3.2.3 DGFET Operation

The operation of the DGFET depends upon the operating characteristics of each FET, specifically the voltages V_{DD1}, V_{D1S}, V_{G2D1} and V_{G1S}, but the actual signal and bias voltages are applied to nodes G1, G2, and D. The internal and external voltages are related as follows:

$$V_{DS} = V_{D1S} + V_{DD1} \qquad (3.2.3.1)$$

$$V_{G2D1} = V_{G2S} - V_{D1S} \qquad (3.2.3.2)$$

The exact operating condition of the DGFET is difficult to characterize because the internal voltage at D1 cannot be measured.[14] However, if the I-V characteristics of each FET are plotted on a single graph insight into the operating point of the DGFET can be obtained. Figure 3.2.3.1 shows the overlapping of each FET's I-V characteristics for a constant V_{DS} using the relationship $V_{DS} = V_{D1S} + V_{DD1}$. The corresponding DGFET drain current values are found at the intersection of the two FET curves since the drain currents must be essentially equal under normal operating conditions.

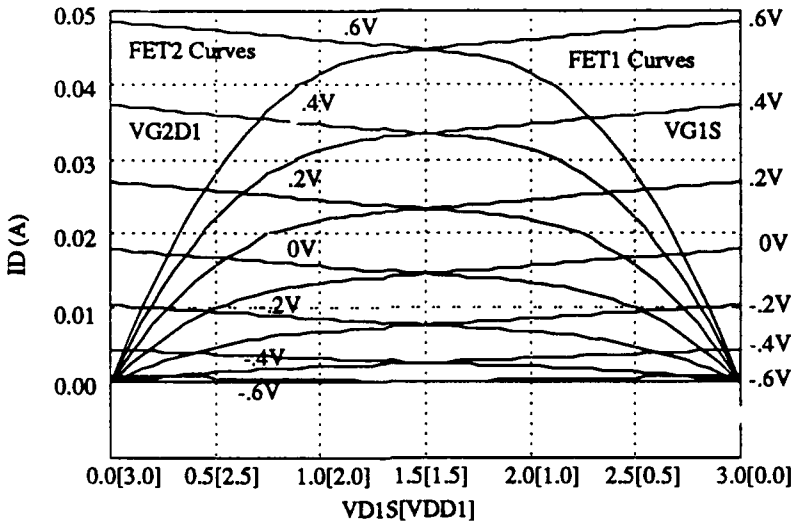

Figure 3.2.3.1 Overlapping I-V characteristics of each FET.

The problem with Figure 3.2.3.1 is that the drain current is a function of both external and internal voltages. A better plot overlays the previous figure with constant V_{G2S} , FET2 drain current curves. Now, by inspection, the individual operating points of the FETs can be found as a function of the actual applied voltages.

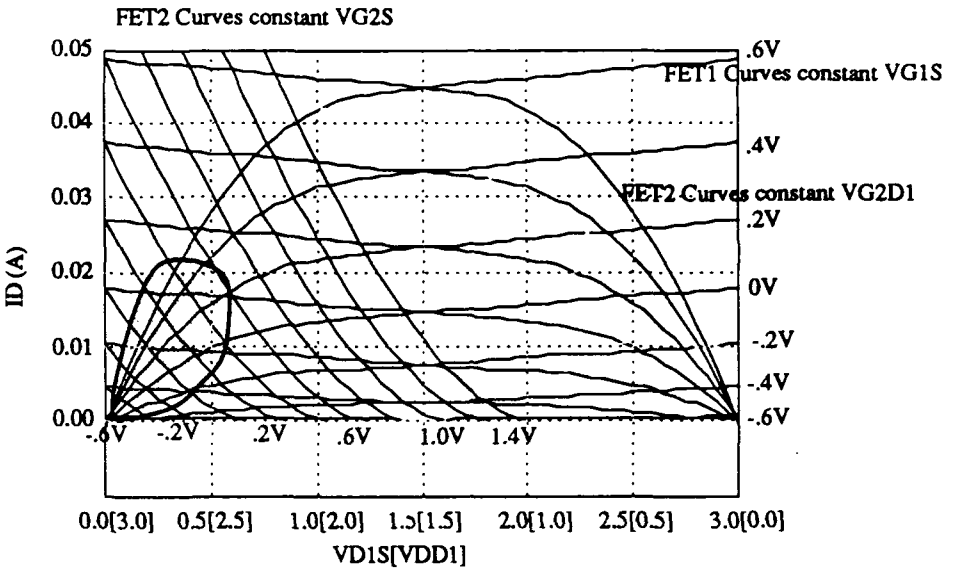

Figure 3.2.3.2 I-V characteristics of each FET as a function of external voltages. (Shaded area represents low noise mixing bias)

3.2.4 DGFET as a mixer

When a DGFET is used as a mixer, typically, the LO and RF signals are applied to the second and first gates respectively. (G2 an G1 of Figure 3.2.1(a)) Although there are several operating points suitable for mixing, Tsironis *et al* [8] have shown that the shaded area in Figure 3.2.3.2 is the desired operating point for a low noise mixer. In this area, the lower FET provides the non-linearities while the upper FET provides IF amplification. Since the drain current is small, low noise operation is expected. Changes in the LO voltage force movement along the knee of the FET1 I-V curves causing non-linear transconductance changes. Figure 3.2.4.1 schematically represents how a low noise DGFET mixer can be thought of as a mixing stage and an amplification stage.

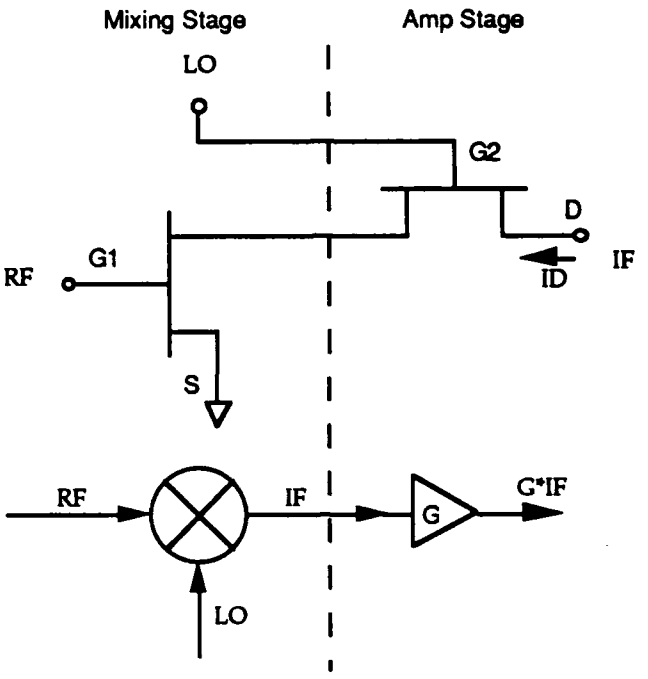

Figure 3.2.4.1 Schematic of LNM DGFET operation

Compared to a diode, the DGFET's non-linearities are weak and the exact mixing process is not well defined.[10] Tsironis *et al* [8] showed that the non-linear elements of the DGFET are the transconductance, gm; drain-to-source resistance, Rds, gate-to-source capacitance, Cgs; and gate-to-drain capacitance, Cgd of each FET in the model. After measuring these parameters versus the gate voltages, they found that in the low noise mixing mode the dominant non-linearities are contributed by the gm and Rds of the lower FET. In their work, they produced three-dimensional plots of gm and Rds versus V_{G1S} and V_{G2S} clearly showing non-linear behavior that could be exploited to produce mixing. Similarly, Figure 3.2.4.2 is a plot of gate 1 transconductance, gm_1, versus V_{G1S} stepped for constant V_{G2S} voltage for a QED/A 300 μm depletion-mode DGFET; however, like Tsironis' plots, they may show non-linearities but do not clearly indicate a optimum bias that would optimize "mixing" or conversion gain.

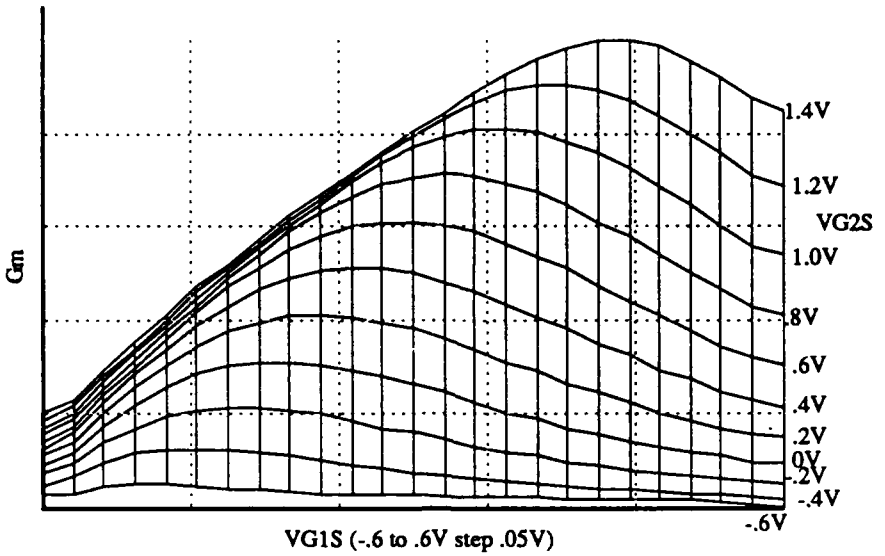

Figure 3.2.4.2 Gate 1 transconductance versus VG1S.

3.2.5 Conversion Gain Optimum Bias

Obviously, the performance of a DGFET mixer depends on the gate bias, V_{G1S} and V_{G2S}; the bias must provide a set point which promotes some multiplication of v_{lo} and v_{rf}. Furthermore, changes in both gate voltages must cause changes in the drain current. It seems intuitive that for mixing to occur, the partial derivative of I_D with respect to the gate biases must be non-zero. If either were zero it would be impossible to get an IF product. Figures 3.2.5.1 and 3.2.5.2 are plots of I_D versus gate bias.

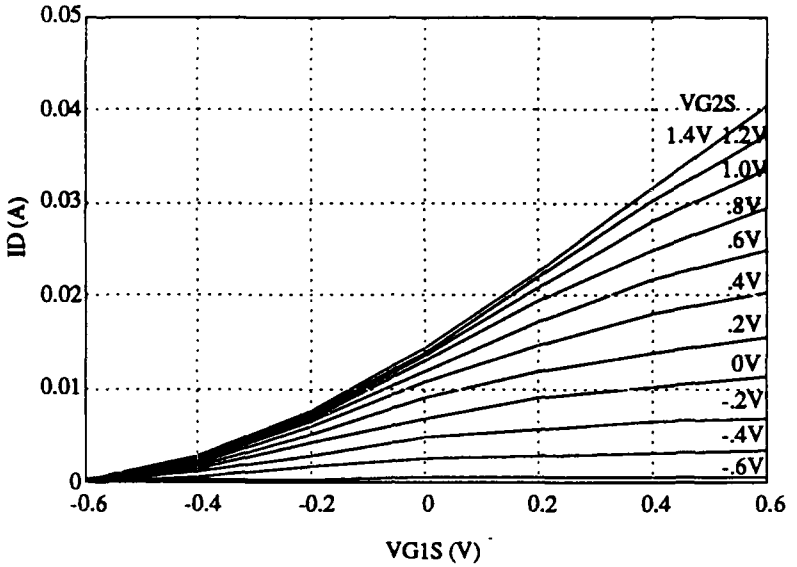

Figure 3.2.5.1 DGFET ID versus VG1S (VDS=3.0V).

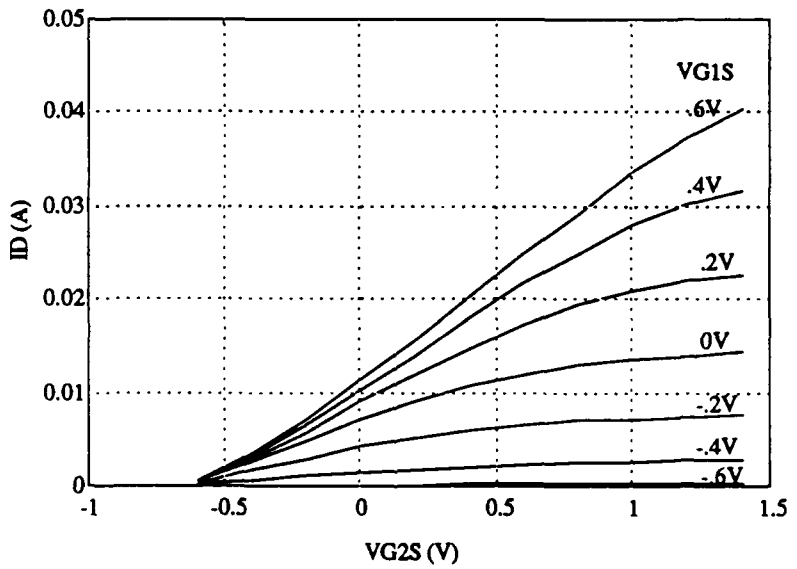

Figure 3.2.5.2 DGFET I_D versus V_{G2S} (V_{DS}=3.0V).

Again, intuitively, the maximum amount of IF power via I_D through a load might be a function of the gradient of the I_D surface (Figure 3.2.5.3) and the magnitude of the current.

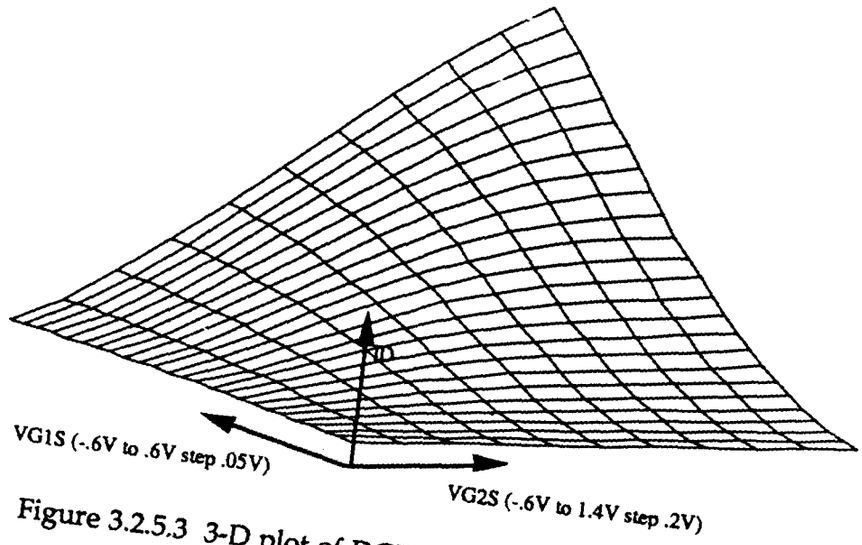

Figure 3.2.5.3 3-D plot of DGFET I_D versus V_{G2S} (V_{DS}=3.0V).

Recall that the gradient of I_D would be

$$\nabla I_D = gm_1\hat{x} + gm_2\hat{y} \qquad (3.2.5.1)$$

where

$$gm_1 = \frac{\partial I_D}{\partial V_{G1S}} \qquad (3.2.5.2)$$

$$gm_2 = \frac{\partial I_D}{\partial V_{G2S}} \qquad (3.2.5.3)$$

if V_{G1S} is plotted on the x axis and V_{G2S} on the y axis. Figure 3.2.5.4 represents the constant I_D contours of Figure 3.2.5.3 overlaid with the gradient vectors evaluated at various bias points.

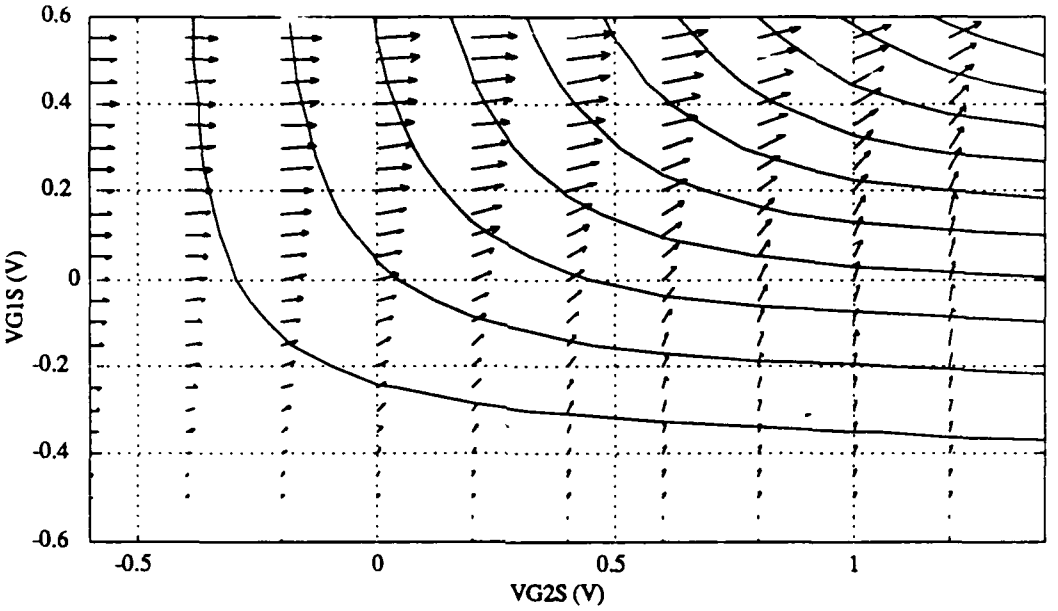

Figure 3.2.5.4 Constant I_D contours and gradient (I_D) versus gate bias

It would be convenient if the maximum gradient reflected an optimum bias; however, zero gm_1 or gm_2 could still produce a very large gradient but no mixing. Instead, recalling the mixer/post IF amp model of the low noise DGFET mixer, gm_1 is proportional to the conversion gain of the mixing stage and gm_2 is proportional to the gain of the post amp stage. Then the optimum bias may exist where the product of gm_1 and gm_2 is the largest. If G_T is defined as the product of the two transconductances (Equation 3.2.5.4), a three-dimensional plot of G_T clearly shows a ridge representing maximum G_T for a given bias and I_D.

$$G_T = gm_1 \cdot gm_2 \qquad (3.2.5.4)$$

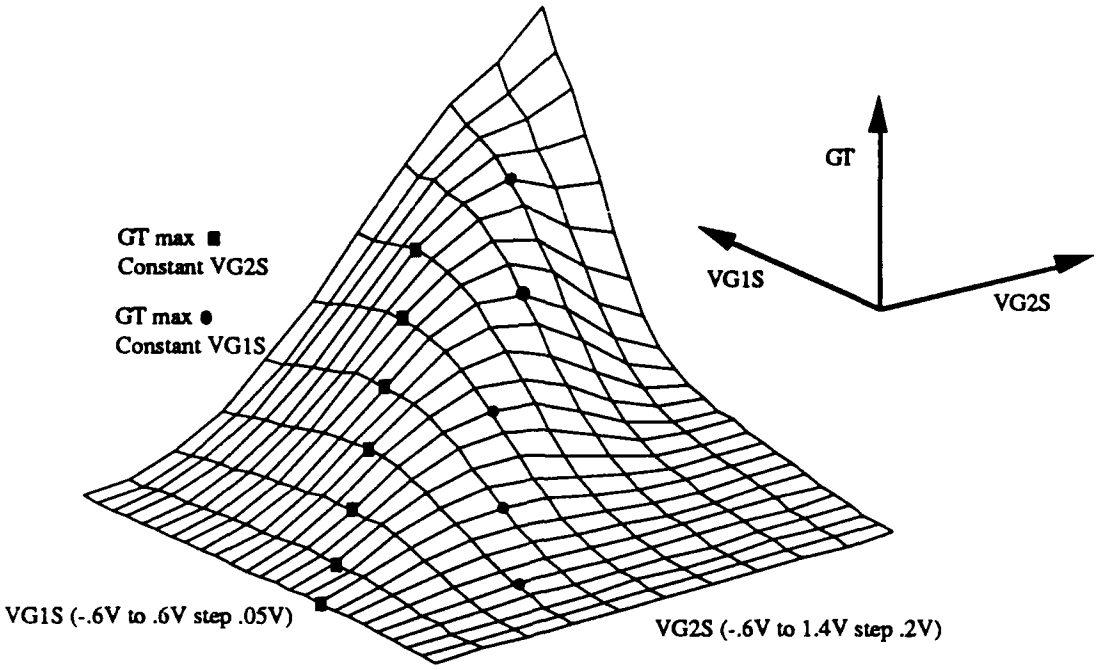

Figure 3.2.5.5 G_T versus gate bias (V_{DS}=3.0V).

For a given drain current, V_{G2S} would try to settle where G_T was a maximum for constant V_{G1S} (black squares) and V_{G1S} would try to settle where G_T was a maximum for constant VG2S (black circles). It follows that an "optimum" bias would occur somewhere between the two G_T max lines, in other words on the ridge of the surface. In order to verify if optimum biases occur on this ridge, a test circuit simulation was developed. This circuit simulates the measurement of a DGFET device with a spectrum analyzer through bias-tees and 50Ω terminations. (Figure 3.2.5.6).

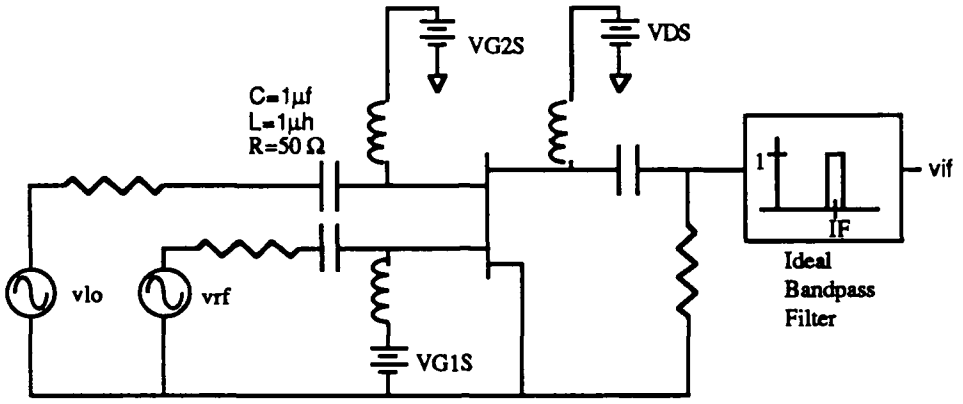

Figure 3.2.5.6 DGFET test fixture.

With this circuit the optimum V_{G2S} bias (largest conversion gain) was found for a fixed V_{G1S} bias. Figure 3.2.5.7 represents constant G_T contours overlaid with G_T max region (area between G_T max lines) and the optimum biases found through simulation. The simulated results (black triangles) follow along the G_T max region as expected, but are shifted toward the lower V_{G1S} biases. This shift reflects an additional dependance. Not only is the optimum bias a function of the gm product but also the relative power difference between the LO and the RF signals. (The results shown were conducted with -.45 and -16 dBm power levels) Intuitively, it would seem that if the LO power is much larger than the RF power, gm_2 would have more weight than gm1 and the optimum biases would shift toward larger gm_2.

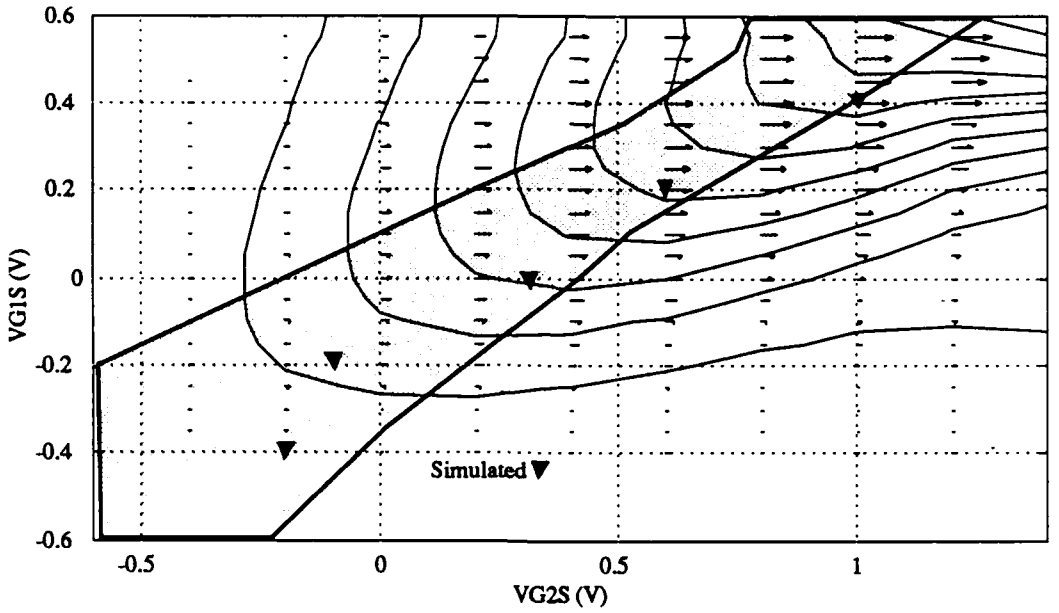

Figure 3.2.5.7 G_T contours with shaded G_T max region.

Therefore, the work of characterizing a DGFET's bias effect on conversion gain could be significantly changed from a very empirical approach or elaborate parameter characterization to a straightforward procedure based on I_D measurements. The procedure would be 1) measure a DGFETs I-V characteristics with a curve tracer; 2) develop an mXn matrix of I_D values where the rows and columns represent the gate biases; 3) calculate the components of the gradient; 4) calculate G_T which is the product of the two gradient components; 5) find the G_T max bias region; 6) determine the drain current required to produce the necessary power; 7) follow the I_D contour to the G_T max bias region; and 8) simulate for a cluster of biases in that region with the desired input power levels. With existing software programs, like MATLAB, this procedure is relatively easy. Once the I_D matrix is entered into the computer, G_T max region can be found in a few minutes.

Of course, the actual conversion gain of a mixer depends on factors other than the bias, such as the matching networks and loading; however, all things held constant these biases should provide the most IF component in the drain current since the device drain current is a function of the applied

voltages at the gates, drain, and source. Determining bias effects on noise and spurious response would be considerably more difficult and not considered in this thesis, and probably better controlled through the matching networks.

3.3 Design and Simulation

With the device models defined and the DGFET operation explained, circuit simulation can begin. The design and simulation of the mixer can be divided into three phases: sub-circuit simulation from schematic, integrated circuit simulation from schematic, and "as built" circuit simulation from the physical layout. The sub-circuit simulation from schematic was the first step in the circuit design; the balun and mixer circuits were designed independently. Next, the sub-circuits were combined to form the overall mixer circuit. During this schematic phase all circuit elements and interconnects are assumed to be "ideal". At the final simulation stage, after the layout was complete, the parasitic effects of the "as built" layout were examined and simulated. (Chapter 4) The remainder of this chapter discusses the design rationale and subsequent circuit schematic simulations. The on chip power is constrained to two power supplies that have been set to +5V and -5V.

3.3.0 Simulation Tools

Since mixing is a non-linear process, the majority of circuit simulations were done using MicroSim's PSpice. PSpice is one of the many SPICE circuit simulators that are based on the SPICE2 circuit simulation program developed at the University of California at Berkeley. SPICE2 based programs have become an accepted standard for analog simulation. [12] Simulating the mixer with PSpice requires time domain analysis and subsequent conversion to the frequency domain with PSpice's FFT function. On the other hand, all the impedance measurements (S- parameters) were done with EEsof's Touchstone using linear models of the devices at the desired bias points as discussed in 3.2.1.

3.3.1 Sub-circuit Schematic Simulations

3.3.1.0 Balun Design and Simulations

The balun needed converts a single-ended signal to a balanced signal. A differential pair configuration is used. (Figure 3.3.1.0.1)

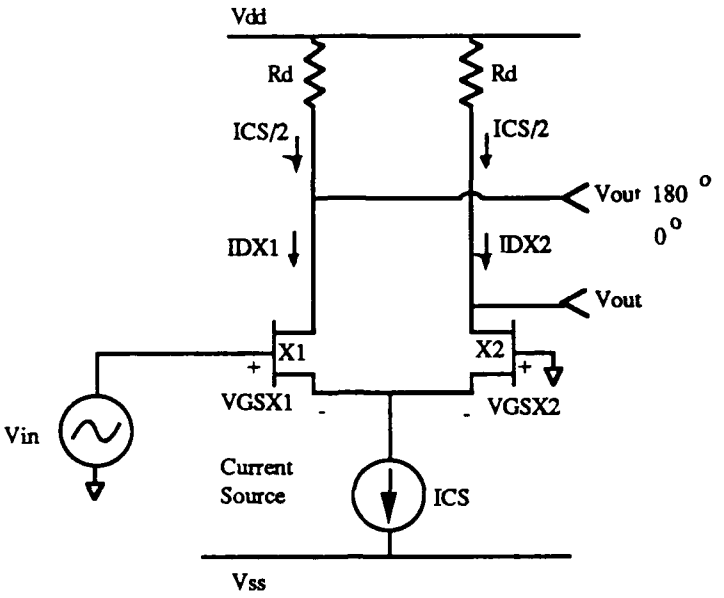

Figure 3.3.1.0.1 Differential pair balun topology

With Vin initially set to zero, since FETs X1 and X2 are identical, I_{CS} divides equally between X1 and X2. With the FET drain currents set at $I_{CS}/2$ and V_{DSX1} and V_{DSX2} set to place the FETs in satuation, V_{GSX1} and V_{GSX2} are forced to take on the value where ICS/2 crosses the FET I-V curves. (Figure 3.3.1.0.2)

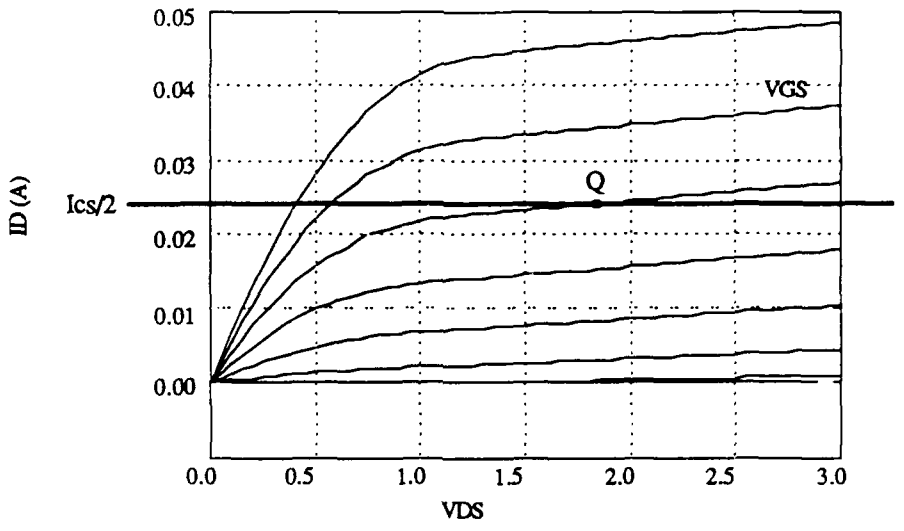

Figure 3.3.1.0.2 Quiescent point of FETs X1 and X2

Now as Vin ramps upward, V_{GSX1} tracks Vin and causes I_{DX1} to increase. Since I_{CS} is constant and $I_{CS} = I_{DX1} + I_{DX2}$, as I_{DX1} increases, I_{DX2} decreases; subsequently, Vout 180° ramps down while Vout 0° ramps up creating a balanced signal. The performance of the balanced mixer depends on the balun's ability to maintain amplitude and phase balance. An imbalance may add power to unwanted frequencies. When designing the balun, there are three major design considerations: the type of current source, the size and type of the differential pair, and the load resistances, R_d.

The I-V characteristics of an "ideal" current source would be perfectly flat for all voltages, representing an infinite impedance. By fixing V_{GS} and operating in the saturation region a single FET can be used as a current source. As seen by the I-V characteristics of single FET current sources using TriQuint's three types of FETs. (Figure 3.3.1.0.3) From the slope of the curves, it can be seen that the M-FET offer the highest output resistance.

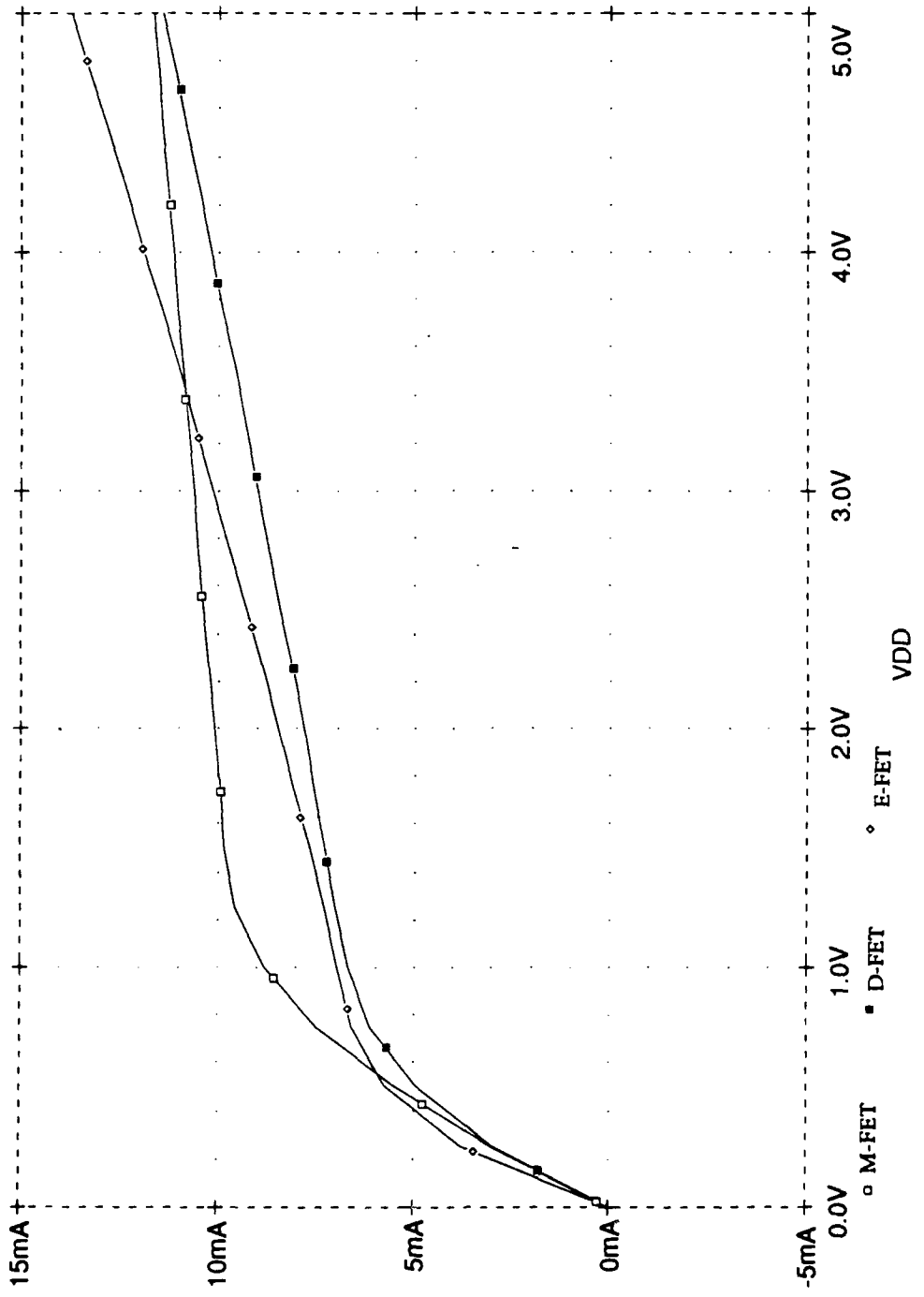

Figure 3.3.1.0.3 TriQuint FET current sources I-V curves

The M-FET offers two other advantages. As with the D-FET since the M-FET is a depletion-mode device, shorting the gate and source of the device is a very convenient way of fixing V_{GS}. Also, the M-FET provides the most current per unit device width. For these reasons, M-FETs are used for all current sources. The final current source configuration is shown in Figure 3.3.1.0.4.

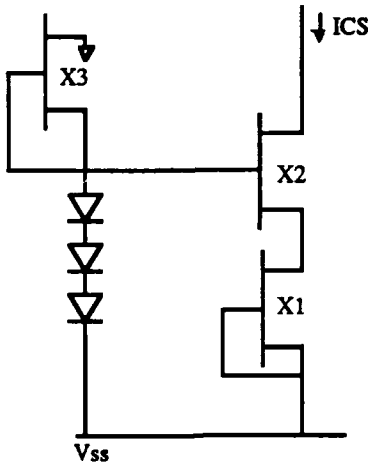

Figure 3.3.1.0.4 M-FET current source configuration.

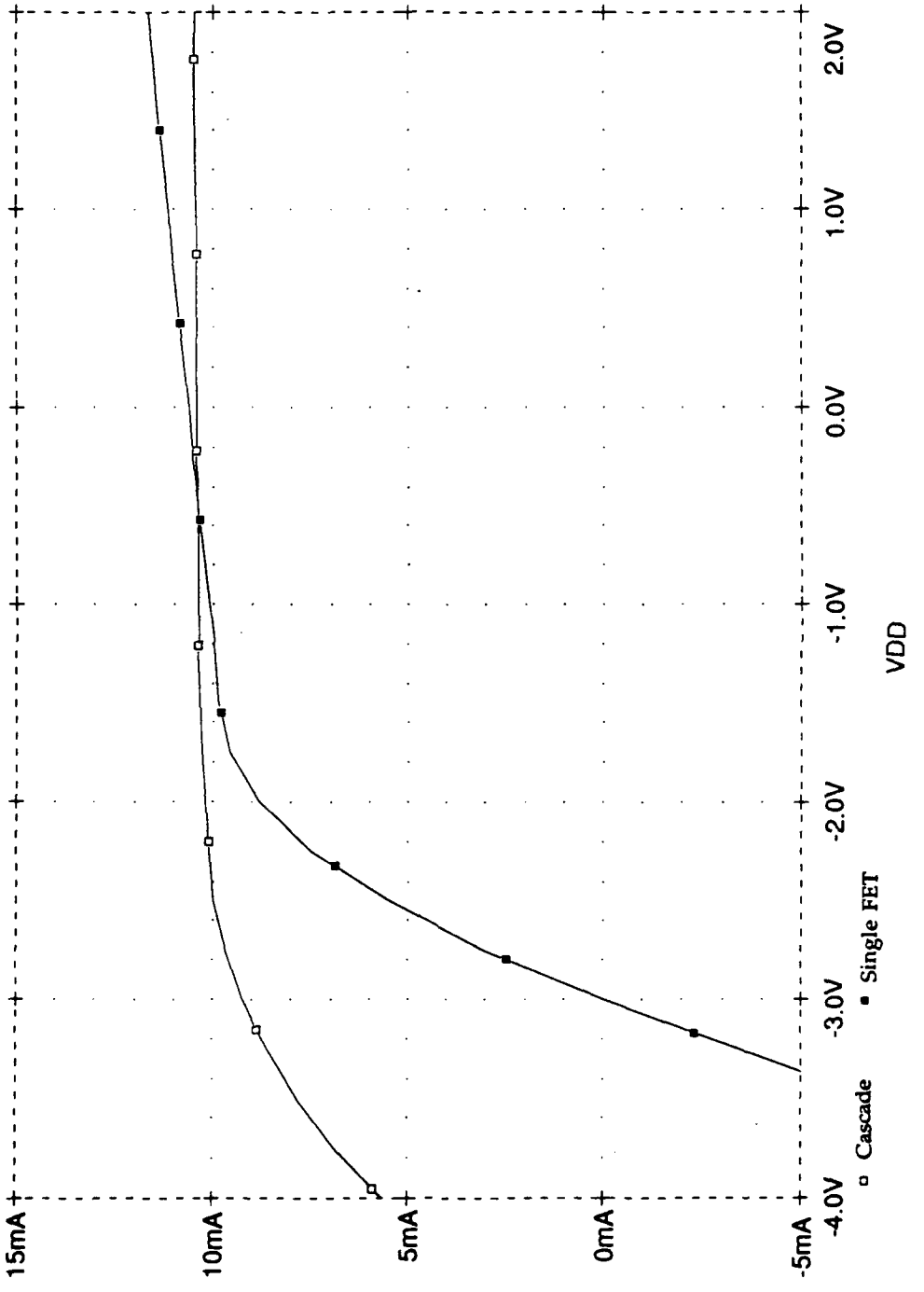

Figure 3.3.1.0.5 Current source I-V characteristics.

This topology offers higher output resistance than a single device. Essentially, FET X2 buffers FET X1. X1 sets the current of the overall current source. Since X2 and X1 are identical in size and type, V_{GSX2} settles very close to zero mimicing V_{GSX1}. The diode stack keeps V_{DSX1} above the knee in the saturation region. Now X2 absorbs any voltage fluctuations at the output of the current source (in the form of V_{DSX2} changes), thus, buffering X1 from any pertubations. Figure 3.3.1.0.5 compares the single M-FET and the cascade topology and the higher output impedance can be seen.

Selection of the balun's differential pair FETs was based on the transconductance of the devices. E-FET, D-FET, and M-FET differential pairs were all simulated (Figure 3.3.1.0.6) at the same bias current and percentage of the maximum saturation current, Idss. Arbitrarily, 15mA was choosen as the bias current and the FETs were scaled to produce a bias at .5 Idss. The resistor values were chosen at 267 Ω to provide a V_{DS} bias of 3V. As Vin ramped from -1.7V to 1.7V and the current through each resistor was measured. (Figure 3.3.1.0.7)

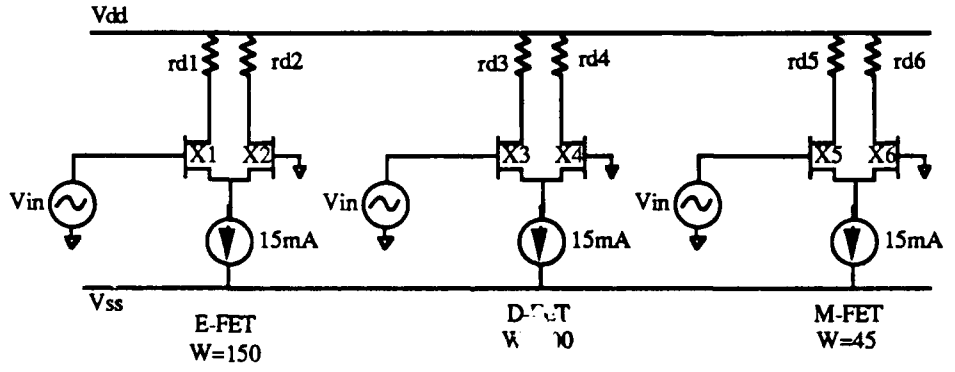

Figure 3.3.1.0.6 TriQuint FET differential pair simulation schematic

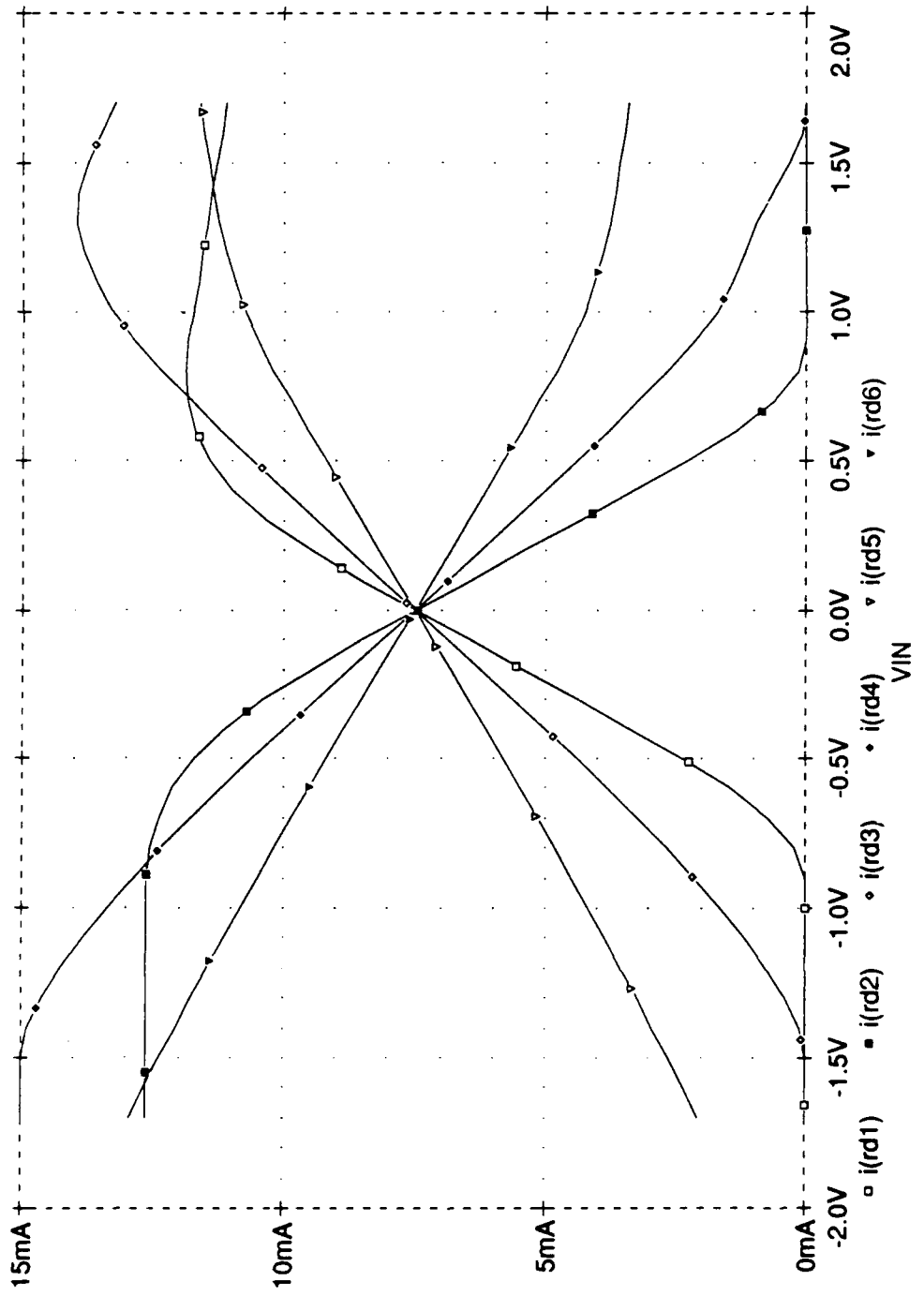

Figure 3.3.1.0.7 TriQuint FET differential pair simulation results

From Figure 3.3.1.0.7, the E-FET curves (denoted by black squares) are the steepest, therefore, offer the greatest potential for gain; but, they also saturate the earliest. Since the linear region of the curves is the desired operating location, a trade-off between the transconductance (slope) and the maximum allowable input voltage (start of saturation) can be seen. In the case of small signals, as used in the mixer, an E-FET differential pair is used in the balun to exploit its potential for gain. Selection of the E-FET will limit the amount of power that should be used to -2 dBm since higher powers will place voltages in excess of 500 mV at the input and create harmonic distortion. At -16 dBm (100 mV), clearly in the linear region, the second and third order harmonics are 47 dB below the fundamental frequency at 1.575 GHz. When the power is increased to -.5 dBm (600 mV), in saturated region, the harmonics are only 26 dB below the fundamental.

Several criteria influence the selection of the load resistance, R_d. First R_d must provide a bias that places the differential pair into saturation. Next, it must be large enough to provide an adequate voltage at the output, but small enough to provide adequate bandwidth to ensure amplitude and phase balance. To show this, three different values of R_d (267, 85, and 8.5 Ω) were simulated in the E-FET pair circuit of Figure 3.3.1.0.6. Figures 3.3.1.0.8 and 3.3.1.0.9, showing the magnitude and phase frequency response indicate how Rd effects performance. The magnitude responses show slight improvement for lower resistances by the later separation of the curves. The phase response differences are more pronounced. Lower resistances provide a constant 180° phase difference for higher frequencies. It is not the roll off that is the key factor but rather the phase difference between the output. As long as the difference is maintained at 180° the balun works correctly. The final balun configuration will be discussed in the circuit integration section.

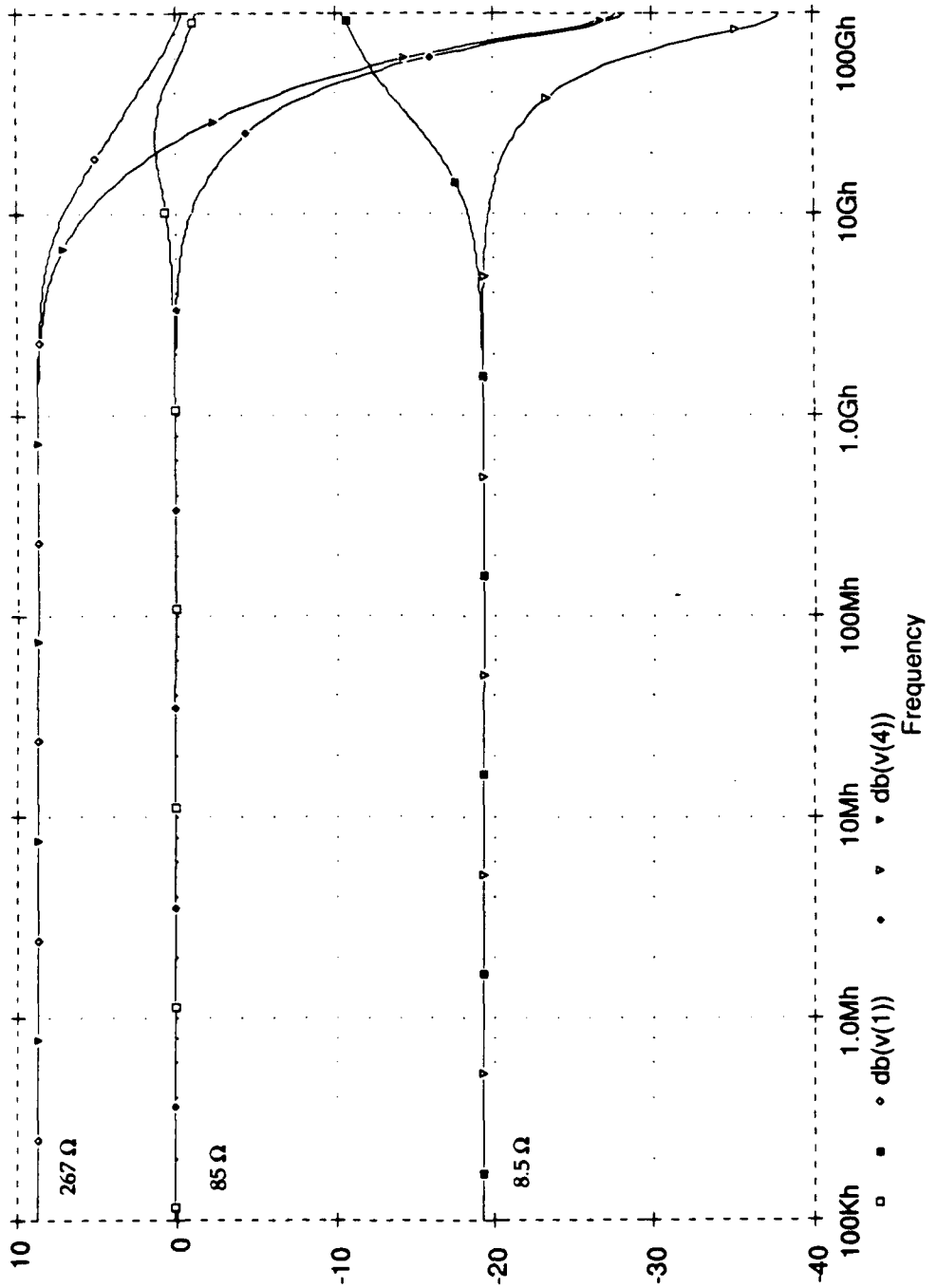

Figure 3.3.1.0.8 Frequency response of E-FET differential pair.

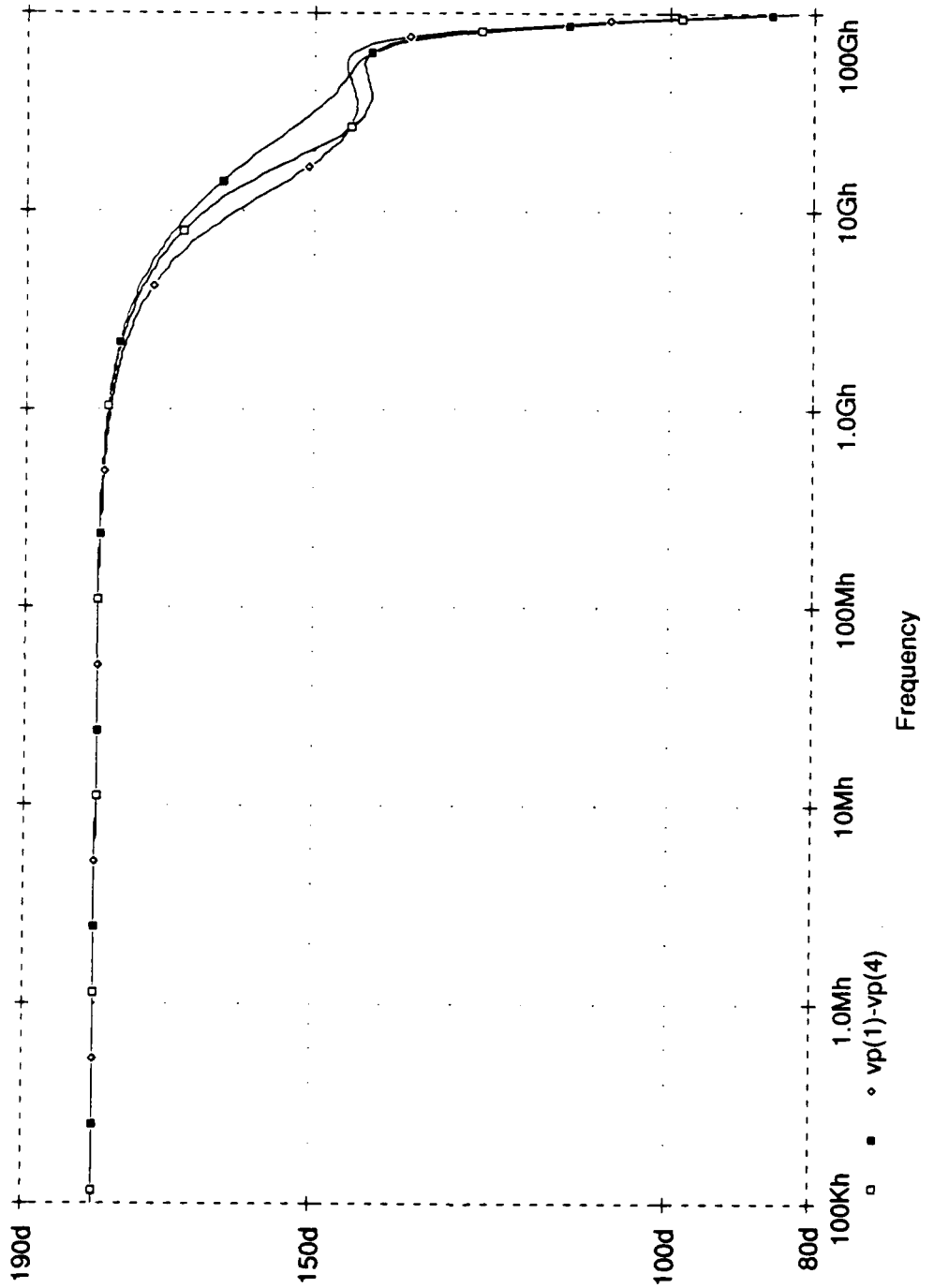

Figure 3.3.1.0.9 Phase difference between E-FET differential pair outputs.

3.3.1.1 Double Balance DGFET Mixer Design and Simulations

By definition a double balanced mixer is two identical single-ended (SE) mixers in parallel. Thus, the first step in the mixer design is to develop a single-ended mixer. A very simple SE DGFET mixer is examined. A 300μm wide D-type DGFET is used as the mixing device. A depletion device is desirable because a zero volt gate bias will provide current which allows for potentially simple bias circuits if necessary. A large 300 μm device is used to ease DGFET modeling as a result of the low drain and source resistances. A D- type is used to keep power consumption relatively low compared to the large current M-FET. Since bias tees at L-band frequencies are too large to provide the device bias on a monolithic circuit, resistive biases were used. The design of the gate bias will be discussed in the integration section, so for now, it is assumed the proper biases and perfectly balanced signals are present at the gates. The load impedance of the mixer is considered to be 50 Ω, and the output is AC coupled to prevent a subsequent stage from affecting the bias.

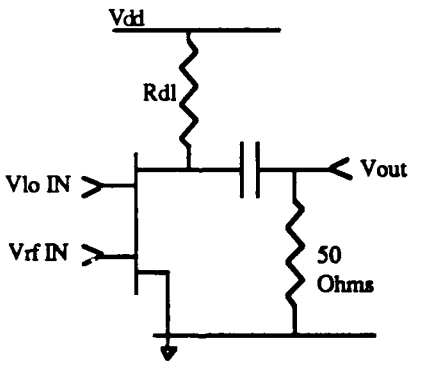

Figure 3.3.1.1.1 SE DGFET mixer

Since low noise is desired, a low DGFET drain current of 7.5mA is selected. From Figures 3.2.5.4 and 3.2.5.7, an optimum bias for that current is around zero volts for both V_{G1S} and V_{G2S}. The drain bias resistor is set to 250 Ω to provide a 3V V_{DS}. The problem with this simple SE configuration is that the 50 Ω termination loads down the drain resistor and considerably dampens the output. As discussed, matching on chip at 173 MHz is impossible with lumped or distributed elements, so a buffer amplifier was used at the output.

(Figure 3.3.1.1.2) As done by Siguira *et al* [2], the buffer replaces a matching network and provides gain to overcome the matching problems. A 300 μm D-FET is used with a 150 Ω drain bias resistor and a large gate bias resistor (1k Ω) to set V_{GS} at zero volts.

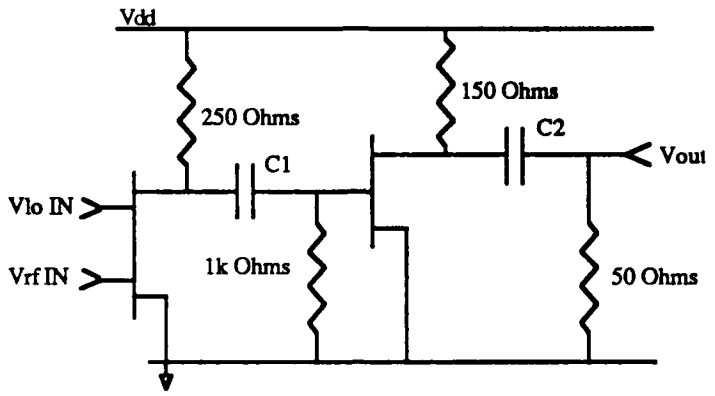

Figure 3.3.1.1.2 SE DGFET mixer with buffer amplifier output stage

Ideally, the capacitors used to provide AC coupling should be as large as possible; however, on chip space available limits their size. Since two interstage capacitors (C1) and one output coupling capacitor (C2) will be needed, C1 is kept to 5 pF and C2 is set to 25 pF.

Before futher discussion of the design of the mixer, it is useful to mention the calculations of the conversion gain and isolation. The conversion gain is calculated based on the following equation:

$$\text{Conversion gain (dB)} = P_{out}\text{ (dBm)} - P_{avail}\text{(dBm)} \qquad (3.3.1.1.1)$$

where P_{out} is the power in the IF component at the load and P_{avail} is the available power in the RF component at the RF port. Available power is defined as the power at the load if the source and load impedances were equal and the system were removed.[21] Figure 3.3.1.1.1 represents at typical system with source (R1) and load (R2) impedances connected to a network.

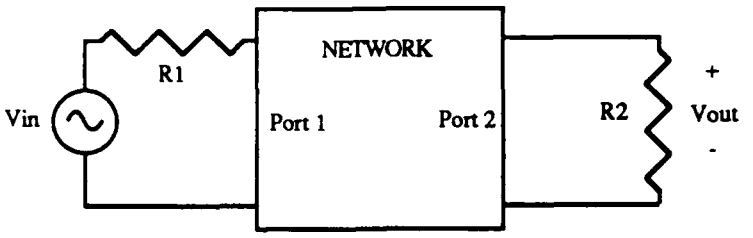

Figure 3.3.1.1.3 Typical system.

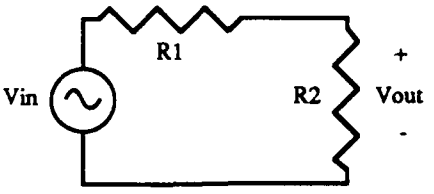

Figure 3.3.1.1.4 Typical system with network removed for available power calculations.

Without the network (Figure 3.3.1.1.4), V_{out} is result of a simple voltage divider.

$$V_{out} = \frac{R_2}{R_1+R_2} V_{in} \qquad (3.3.1.1.2)$$

and if R1 = R2 = 50 Ω , then $P_{avail} = (1/2\ V_{in})^2/50$ watts or in dBm

$$P_{avail} = 10 \log 5(V_{in})^2 \qquad (3.3.1.1.3)$$

However, since Vin is of the form Acos ω̇t, Vin^2 is replace by the time average which is $1/2\ (A)^2$ so the final equation becomes

$$P_{avail} = 10 \log 2.5(A)^2 \qquad (3.3.1.1.4)$$

PSpice represents signals as voltages and currents, not power, so it is useful to have a conversion table of input voltages in mV to power available in dBm. (Table 3.3.1.1.1)

Pwr avail (mV)	Pwr avail (dBm)	Pwr avail (mV)	Pwr avail (dBm)
10	-36.02	525	-1.62
25	-28.06	550	-1.21
50	-22.04	575	-0.83
75	-18.52	600	-0.46
100	-16.02	625	-0.10
125	-14.08	650	0.24
150	-12.50	675	0.57
175	-11.16	700	0.88
200	-10.00	725	1.19
225	-8.98	750	1.48
250	-8.06	775	1.77
275	-7.23	800	2.04
300	-6.48	825	2.31
325	-5.78	850	2.57
350	-5.14	875	2.82
375	-4.54	900	3.06
400	-3.98	925	3.30
425	-3.45	950	3.53
475	-2.49	975	3.76
500	-2.04	1000	3.98

Table 3.3.1.1.1 Available Power Conversion Table mV to dBm (50 Ohm system)

The output power is simply $1/2\ (A)^2/50\ \Omega$ watts or in dBm as Table 3.3.1.1.2 shows.

Pwr out (mV)	Pwr out (dBm)	Pwr out (mV)	Pwr out (dBm)
10	-30.00	525	4.40
25	-22.04	550	4.81
50	-16.02	575	5.19
75	-12.50	600	5.56
100	-10.00	625	5.92
125	-8.06	650	6.26
150	-6.48	675	6.59
175	-5.14	700	6.90
200	-3.98	725	7.21
225	-2.96	750	7.50
250	-2.04	775	7.79
275	-1.21	800	8.06
300	-0.46	825	8.33
325	0.24	850	8.59
350	0.88	875	8.84
375	1.48	900	9.08
400	2.04	925	9.32
425	2.57	950	9.55
475	3.53	975	9.78
500	3.98	1000	10.00

Table 3.3.1.1.2 Output Power Conversion Table mV to dBm (50 Ohm system)

The isolation measurements between the RF, LO, and IF ports are identical in nature to the gain measurements. For example, LO/IF isolation in dB is defined as

$$\text{LO/IF Isolation}=P_{avail}(\text{LO}) \text{ at LO port}-P_{out}(\text{LO}) \text{ at IF port} \qquad (3.3.1.1.5)$$

Since the SE mixer is only an intermediate step toward the double balanced mixer only select performance data is examined. First, conversion gain versus LO power is presented in Figure 3.3.1.1.5. For the majority of the performance calculations and simulations the RF power was set to -16 dBm which Draper considered an acceptable value for simulation. With a constant

RF power of -16dBm and no matching networks at any port a maximum of 2.84 dB of conversion gain is acheived with an LO power of .88 dBm. However, as discussed the LO power will be limited to -2 dBm when operating the mixer to prevent harmonic generation in the differential pair. Next, conversion gain versus RF power is presented in Figure 3.3.1.1.6. Since simulation time for these types of calculations is extensive the LO power is stepped only three times (-16, -6.5 and -2 dbm) spanning the maximun LO power to the lowest expected possible LO power. The RF and LO power combination affect the flatness of the gain curves. Without any automatic gain control (AGC), it is desireable to operate on a flat portion of the curves so that unwanted mixing does not occur due to any RF signal power fluxuations. With AGC, the flatness becomes less important.

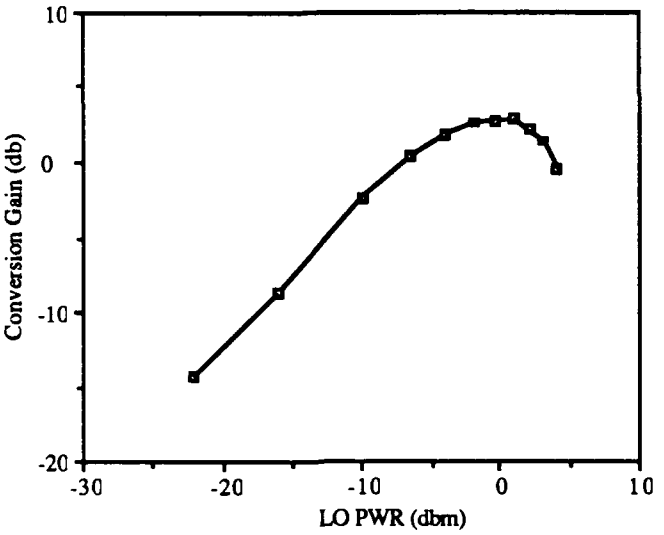

Figure 3.3.1.1.5 SE mixer Conversion Gain versus LO power. (RF power =-16dBm)

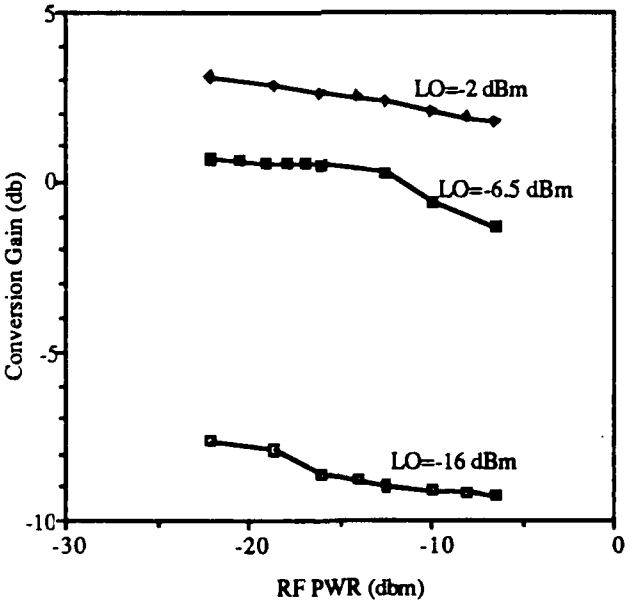

Figure 3.3.1.1.6 SE mixer Conversion Gain versus RF power. (RF power =-16dBm)

Finally, a look at the spectral output of the mixer shows large LO and RF signals that must be suppressed. The frequency products present at a maximum LO power of -2 dBm and an RF power of -16 dbm are listed in Table 3.4.1.1.3.

SE Mixer Frequency Products		Vlo= mV, dBm>	500	-2.04
		Vrf=mV, dBm>	100	-16.02
Product (m,n)	Frequency GHz	Pwr out (mV)	Pwr out (dBm)	Relative to IF (dB)
(1,-1)	0.173	67.5	-13.41	0.00
(2,-2)	0.346	8.3	-31.62	-18.20
(3,-3)	0.519	6	-34.44	-21.02
(-1,2)	1.229	16.3	-25.76	-12.34
(0,1)	1.402	699.1	6.89	20.30
(1,0)	1.575	105.2	-9.56	3.85
(2,-1)	1.748	13	-27.72	-14.31
(-1,3)	2.631	9	-30.92	-17.50
(0,2)	2.804	56.5	-14.96	-1.55
(1,1)	2.977	11.9	-28.49	-15.08
(2,0)	3.150	5.2	-35.68	-22.27
(3,-1)	3.323	2	-43.98	-30.57
(0,3)	4.206	9.6	-30.35	-16.94
(1,2)	4.379	7	-33.10	-19.68
(2,1)	4.552	2.5	-42.04	-28.63
(3,0)	4.725	2	-43.98	-30.57

Table 3.4.1.1.3 Table of mixing products

By placing two SE mixers in parallel, the double-balanced mixer is realized. (Figure 3.3.1.1.7) Now there are four inputs to accommodate the balanced LO and RF signals. The drains of the buffer FETs are tied together and the two 150 Ω resistors were replaced with one 75 Ω resistor to provide identical bias.

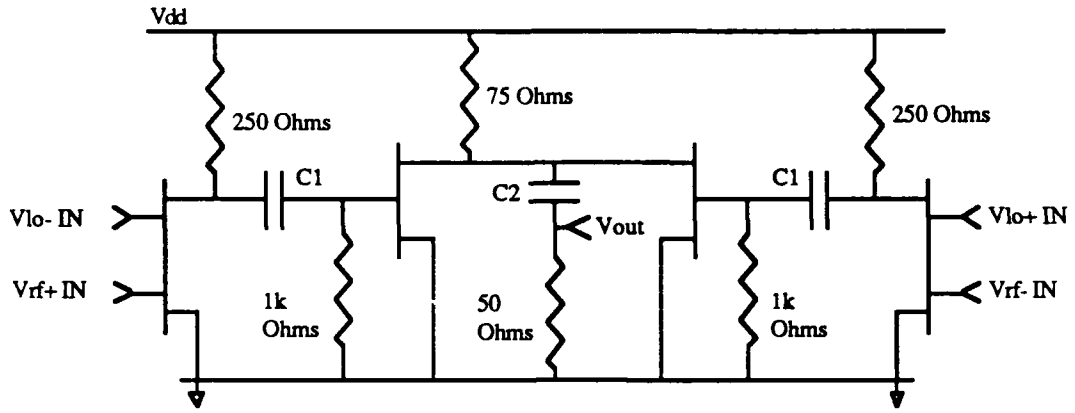

Figure 3.3.1.1.7 Double balanced mixer schematic

The gain characteristics of the double balanced mixer (Figure 3.3.1.1.8) are very similar to that of the single ended mixer; a maximum of 3.05 dB is achieved at an LO power of -2 dBm. Since the balanced mixer requires two inputs it really takes twice the power to achieve the same output power as the SE mixer; however it is not unreasonable to expect unity gain from the active balun. The RF power effects on the gain for the same LO power levels as before are also similar to that of the SE mixer. (Figure 3.3.1.1.9)

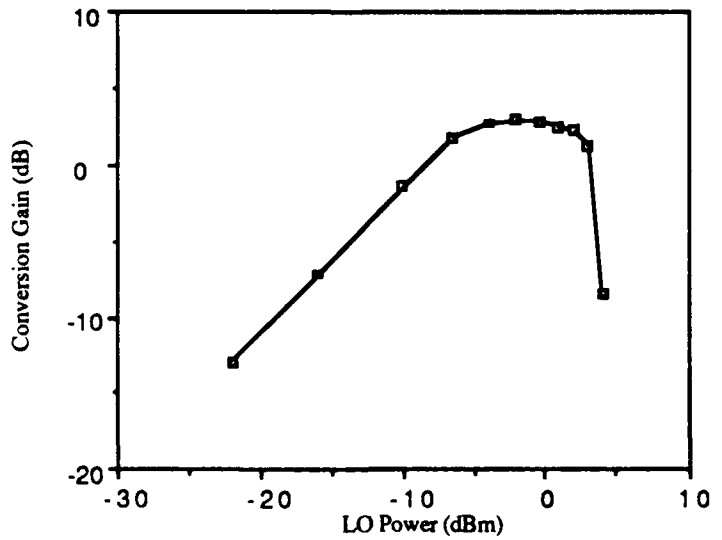

Figure 3.3.1.1.8 DB Mixer Conversion Gain versus LO Power.

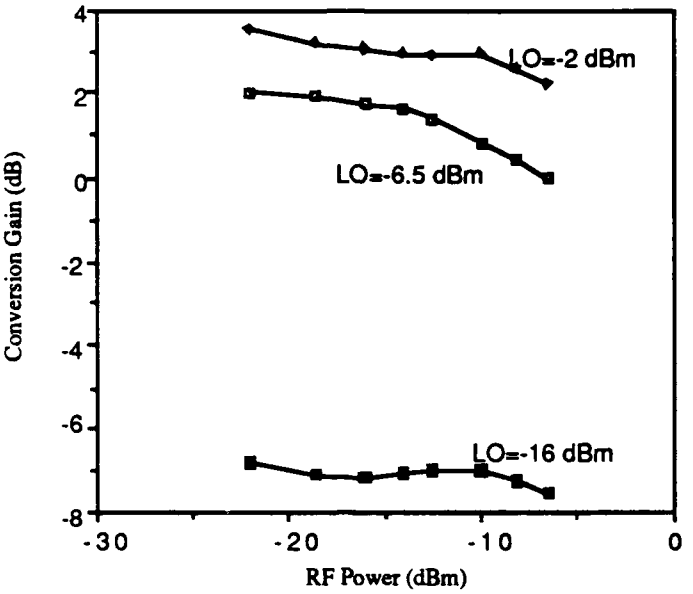

Figure 3.3.1.1.9 DB Mixer Conversion Gain versus RF Power.

Table 3.3.1.1.4 lists the spurious response of the DB mixer versus the LO power levels that produce near unity gain or above. Figure 3.3.1.1.10 graphically represents the spurious response graphically and Figure 3.3.1.1.11 represents the relative power levels compared to the IF power. As expected, the double balanced mixer suppresses the odd harmonics. All of the frequency products between 1.229 and 1.748 GHz are 30 dB below the IF signal. A more useful representation of the mixer's spurious response is shown in Figures 3.3.1.1.12 and 3.3.1.1.13. The frequency axis has been scaled in terms of the intermediate frequency and truncated to 10 IF. The higher frequency spurs are easier to suppress on chip and are considerablely less important. Now, it is easy to see that the (2,-2) spur at 346 MHz has enough power to be significant. Since (2,-2) suppression decreases as the LO power increases, there is a trade off between gain and (2,-2) suppression. Finally, to show how well balancing suppresses the odd harmonics, the spurious responses of the single ended and double balanced mixers, Figures 3.3.1.1.14 and 3.3.1.1.15, are placed next to each other. In this case, balancing provided 50 dB more LO suppression. On the other hand, the DB mixer amplified the second order harmonics, but they are over a decade from the IF and can be suppressed on

chip. Looking at the frequencies up to 10 IF the balanced mixer topology clearly provides much better suppression than the SE mixer. (Figure 3.3.1.1.16)

The important isolation parameters of any mixer are the LO/IF and LO/RF isolation. From Figure 3.3.1.1.12, the LO/IF isolation is almost 40 dB with a perfectly balanced input. Figure 3.3.1.1.18 shows that the DGFET provides 22 dB of LO/RF isolation by its construction alone. (i.e. no filtering)

DB Mixer Frequency Products RF = -16 dBm		LO = -10 dBm	LO = -6.5 dBm	LO = -4 dBm	LO = -2 dBm
Product (m,n)	Frequency GHz	Pwr out (dBm)	Pwr out (dBm)	Pwr out (dBm)	Pwr out (dBm)
(1,-1)	0.173	-17.39	-14.28	-13.19	-12.97
(2,-2)	0.346	-41.37	-30.54	-30.54	-26.65
(3,-3)	0.519	-47.72	-45.92	<-46	-35.04
(-1,2)	1.229	<-50	<-46	<-43	<-42
(0,1)	1.402	<-50	<-46	<-43	<-43
(1,0)	1.575	<-50	<-46	<-43	<-43
(2,-1)	1.748	<-50	<-46	<-43	<-43
(-1,3)	2.631	<-50	-51.94	-39.37	-32.62
(0,2)	2.804	-24.11	-17.05	-12.26	-8.58
(1,1)	2.977	-31.41	-27.86	-25.34	-22.58
(2,0)	3.15	-32.62	-31.41	-30.26	-28.94
(3,-1)	3.323	<-56	<-56	<-50	<-50
(0,3)	4.206	<-56	<-56	<-50	<-50
(1,2)	4.379	<-56	<-56	<-50	<-50
(2,1)	4.552	<-56	<-56	<-50	<-50
(3,0)	4.725	<-56	<-56	<-50	<-50

Table 3.3.1.1.4 Table of DB Mixer mixing products

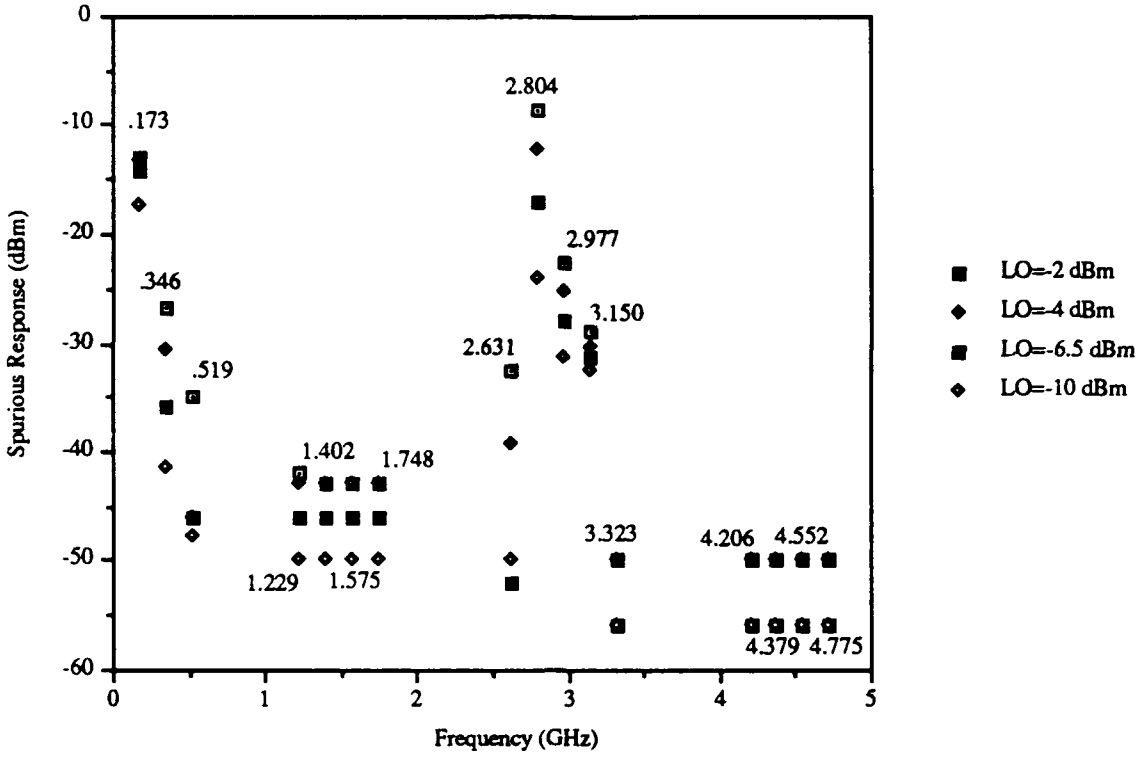

Figure 3.3.1.1.10 Spectrum of DB Mixer Output vs LO Power.

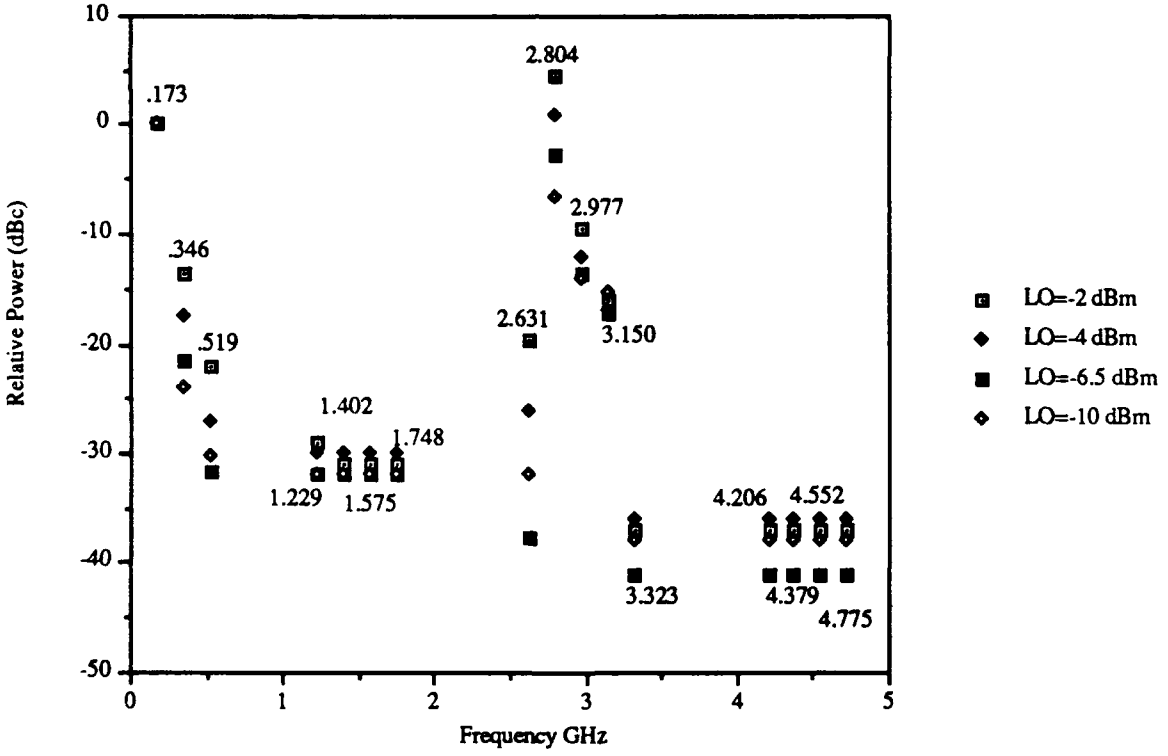

Figure 3.3.1.1.11 Output Power of spurs relative to IF Power.

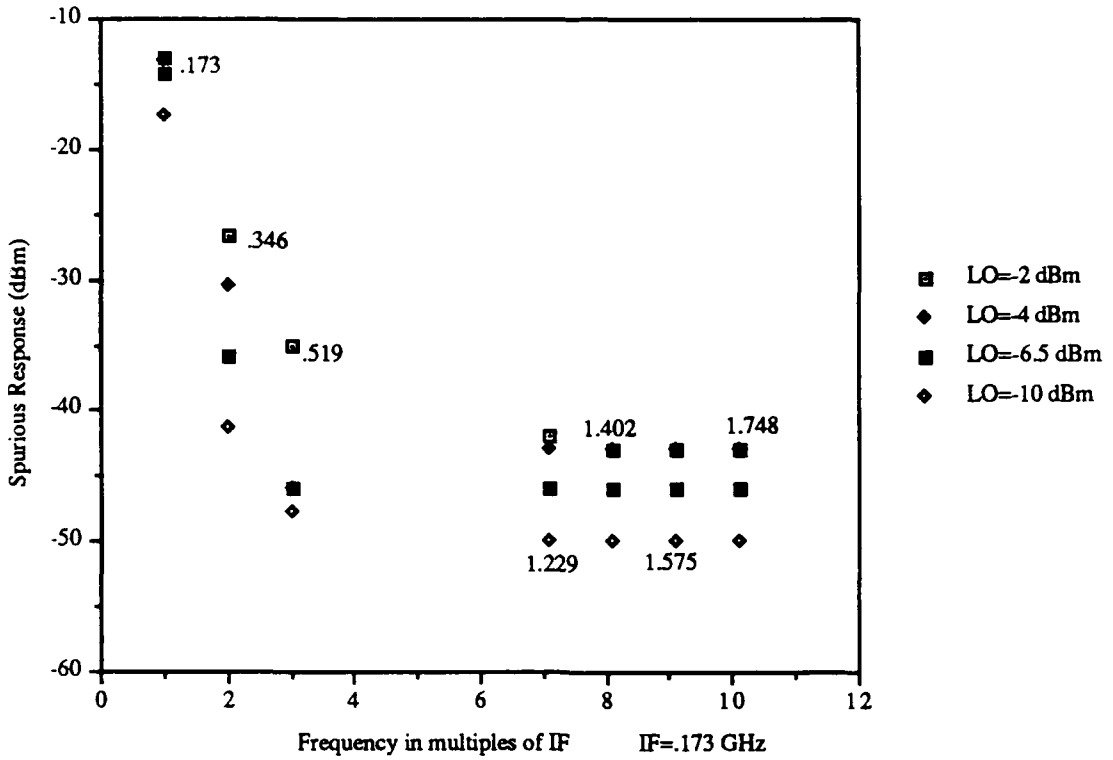

Figure 3.3.1.1.12 Spectrum of DB Mixer Output vs LO Power in terms of multiples of IF.

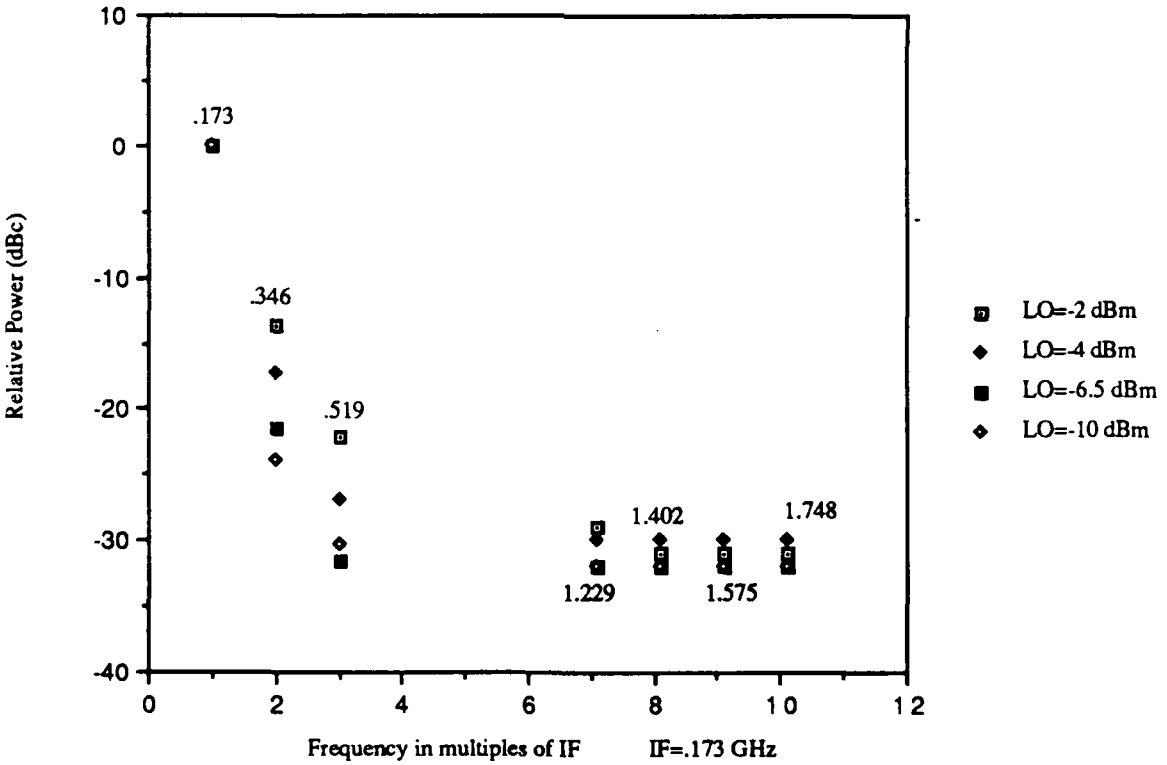

Figure 3.3.1.1.13 Output Power of spurs relative to IF Power in terms of multiples of IF.

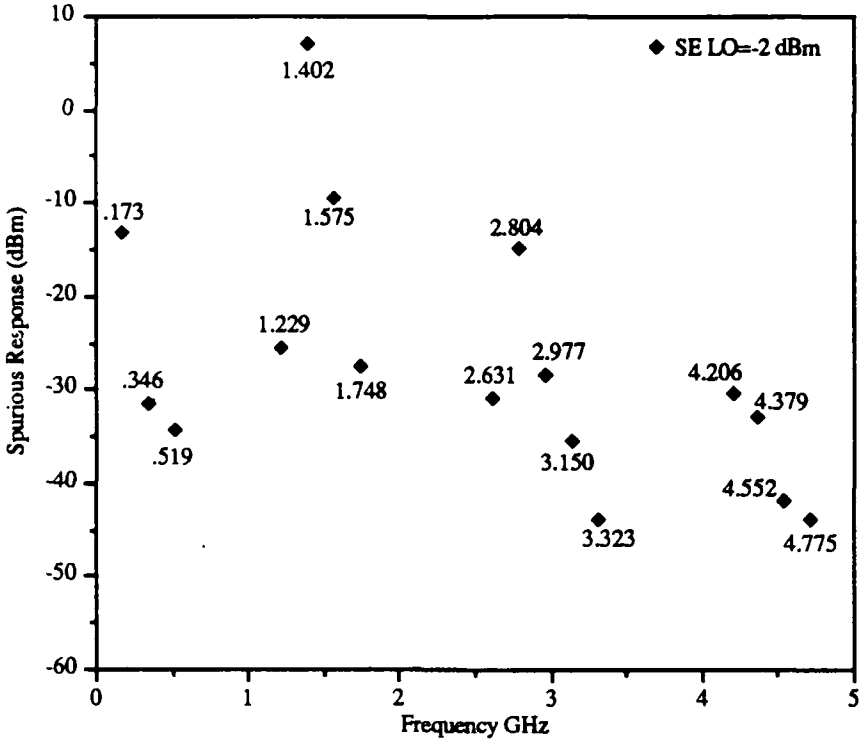

Figure 3.3.1.1.14 SE Spurious Response.

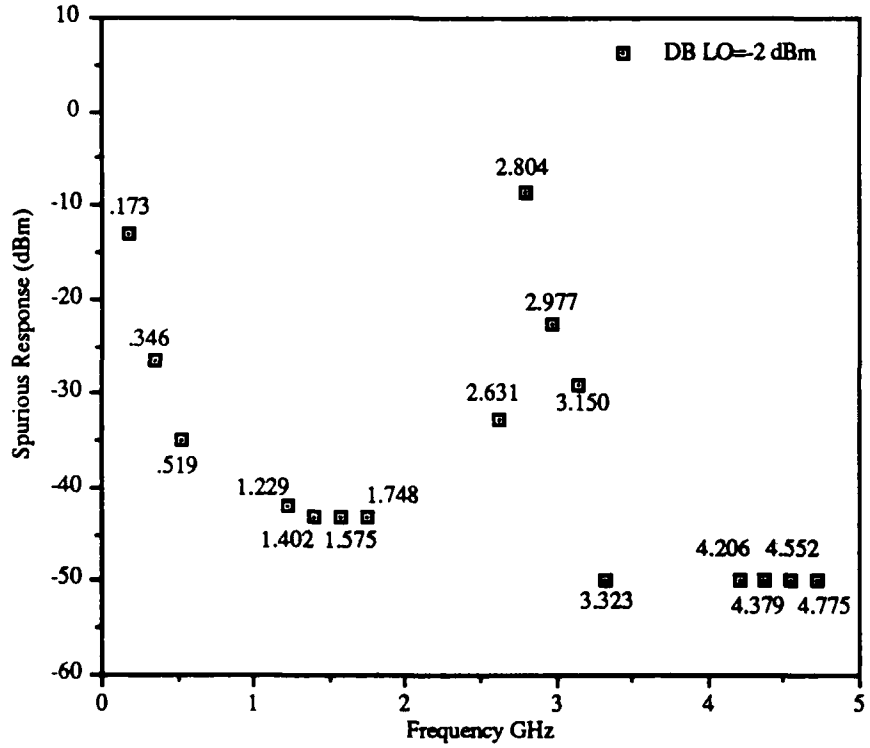

Figure 3.3.1.1.15 DB Spurious Response.

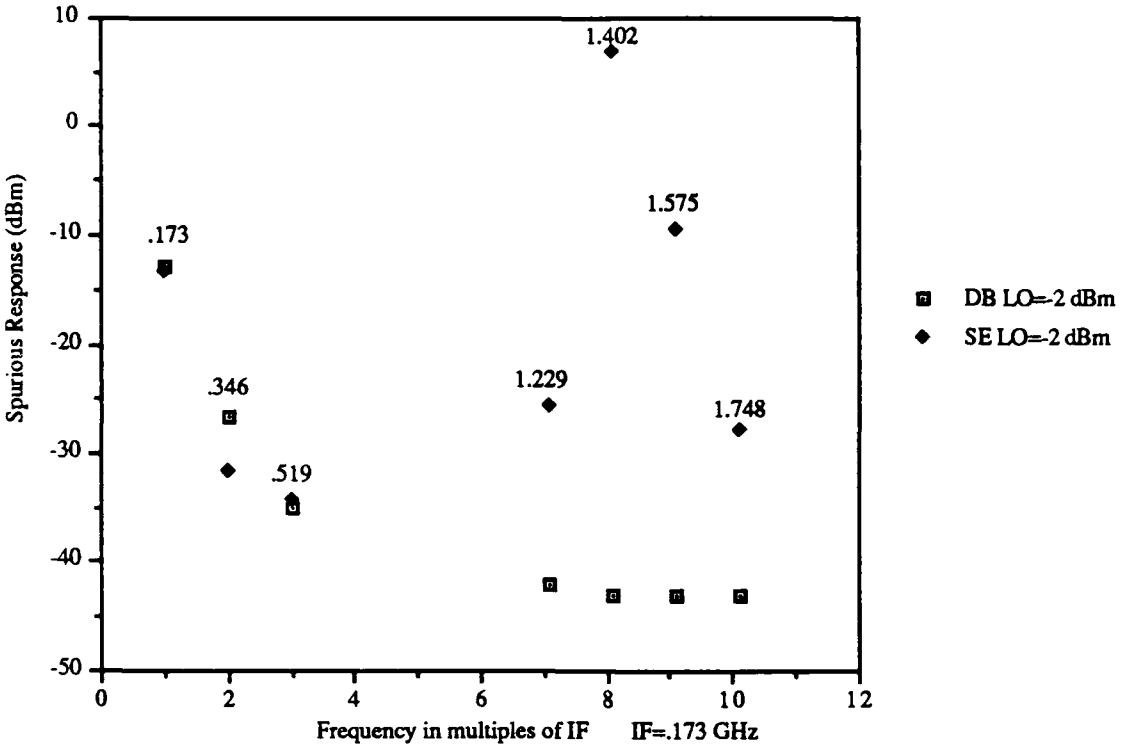

Figure 3.3.1.1.16 DB and SE Spurious Response vs multiples of IF.

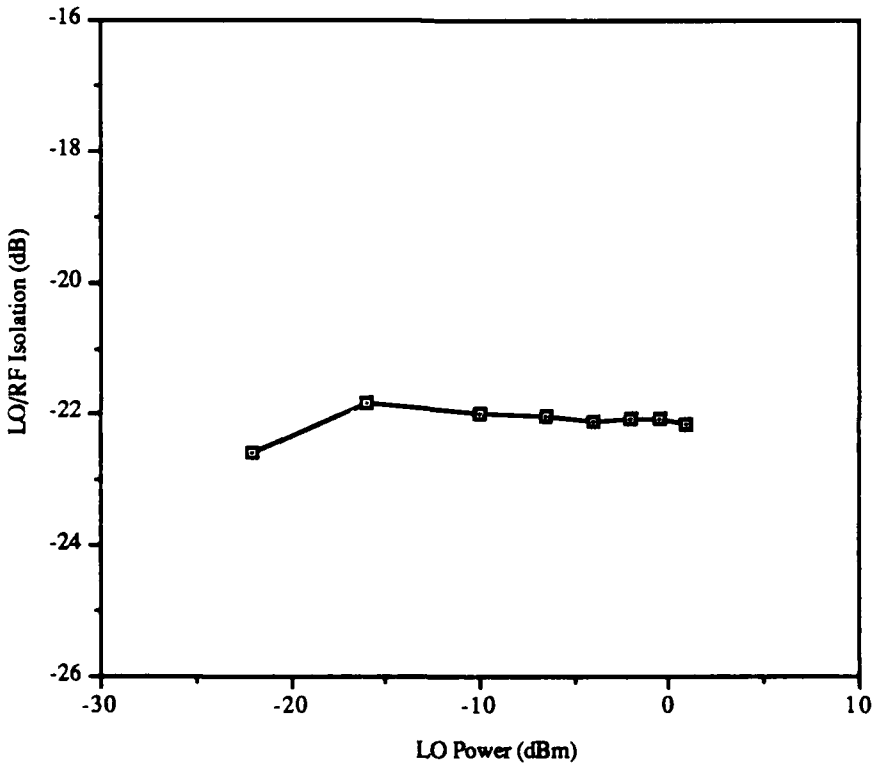

Figure 3.3.1.1.17 LO/RF Isolation through DGFET

3.3.2 Sub-circuit Integration and Circuit Simulations

With the balun and double balanced mixer designed and simulated, the two sub-circuits must be integrated to form the overall mixer circuit.

3.3.2.1 Balun / Double Balanced Mixer Interface

The perferable method of interfacing the the balun and mixer, if size were unconstrained, would be to use AC coupling capacitors and provide separate bias circuitry for each of the four inputs of the double balanced mixer. However, since size is constrained, a level shifting topology (Figure 3.3.2.1.1) is used in order to avoid the space consuming reactive passive elements.

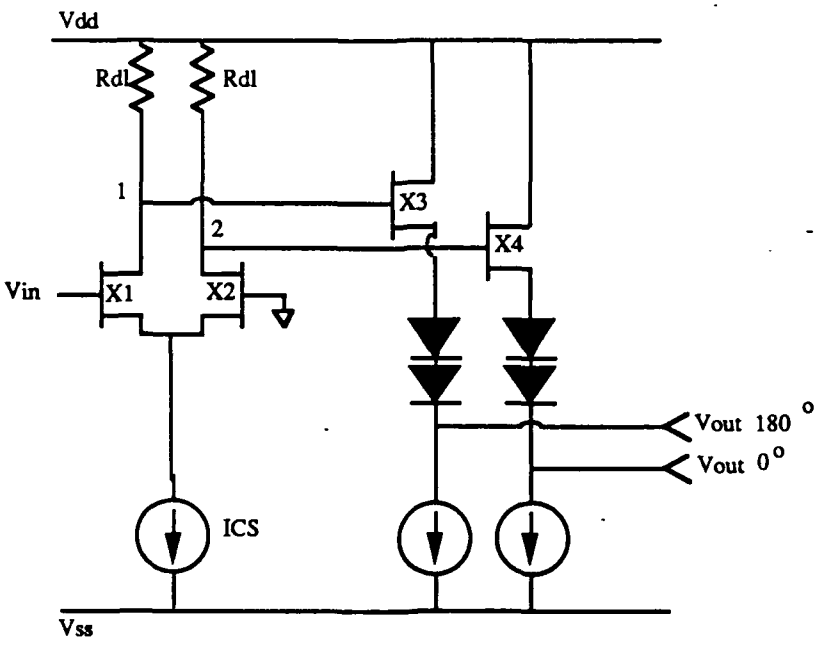

Figure 3.3.2.1.1 Level Shifting Topology

A source follower topology is desirable from a loading stand point because it provides a high impedance to the differential pair and does not load down the output. Cascade current sources (as described in 3.3.1.1) are used and scaled to place the source follower FETs (X3, X4) at .5 Idss. The output bias was set by adjusting the size and number of diodes and adjusting the differential pair bias at points 1 and 2 with Rdl. Two identical baluns are connected directly to the inputs of the double balanced mixer. Figures 3.3.2.1.2 and 3.3.2.1.4 are the final circuit configurations. The balun frequency response, both magnitude and phase, are shown in Figures 3.3.2.1.5 and 3.3.2.1.6. At the expense

of some balance the load resistors of Rdl are set to 578 Ω as the final adjustment to place the proper DC bias at the input to the mixer. The phase difference of the two outputs at 1.575 GHz is 177° and the amplitude difference is 2.8 percent. The harmonic distortion at 1.575 GHz remains good, both the second order and third order harmonics are below 45 dB at -16 dBm input power and degrades to below 22 dB at an input power of -.5 dBm.

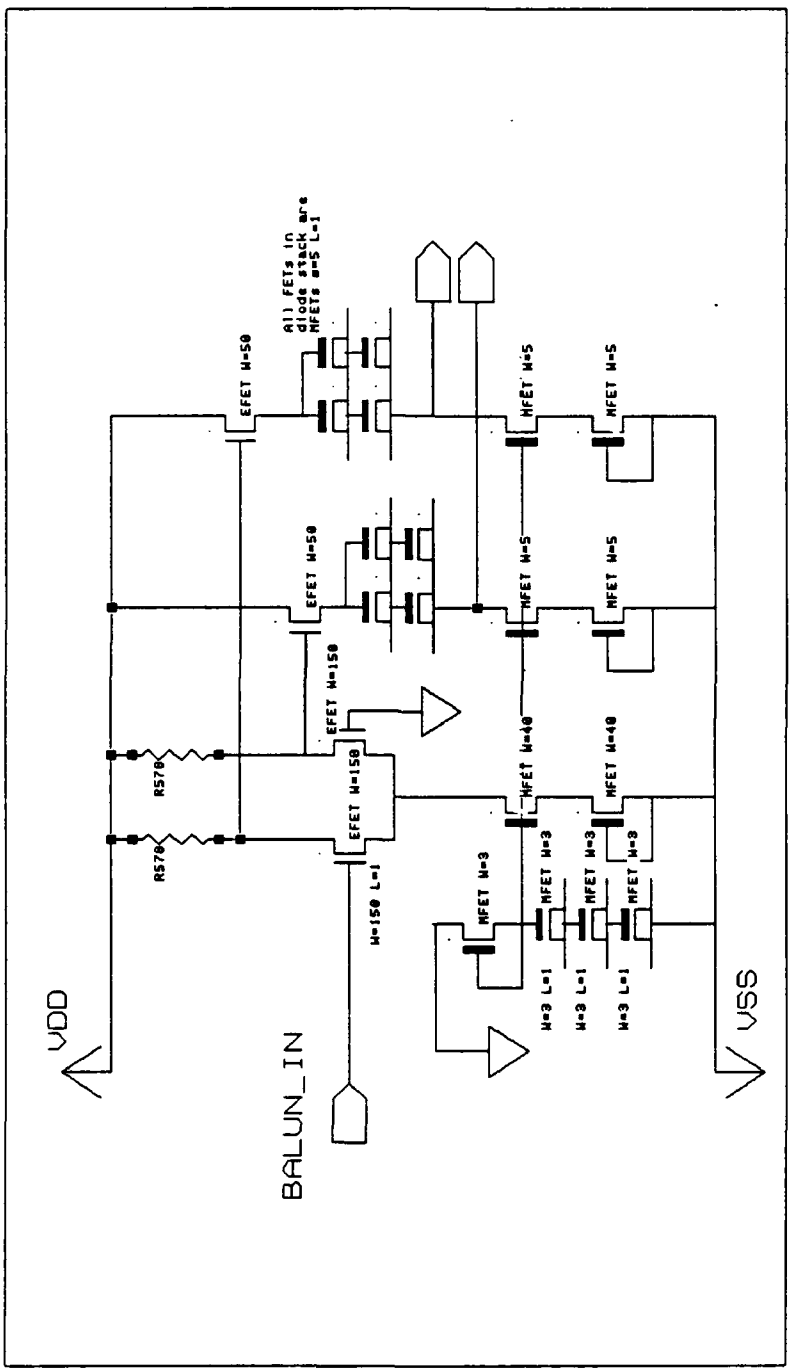

Figure 3.3.2.1.2 Final Balun Configuration

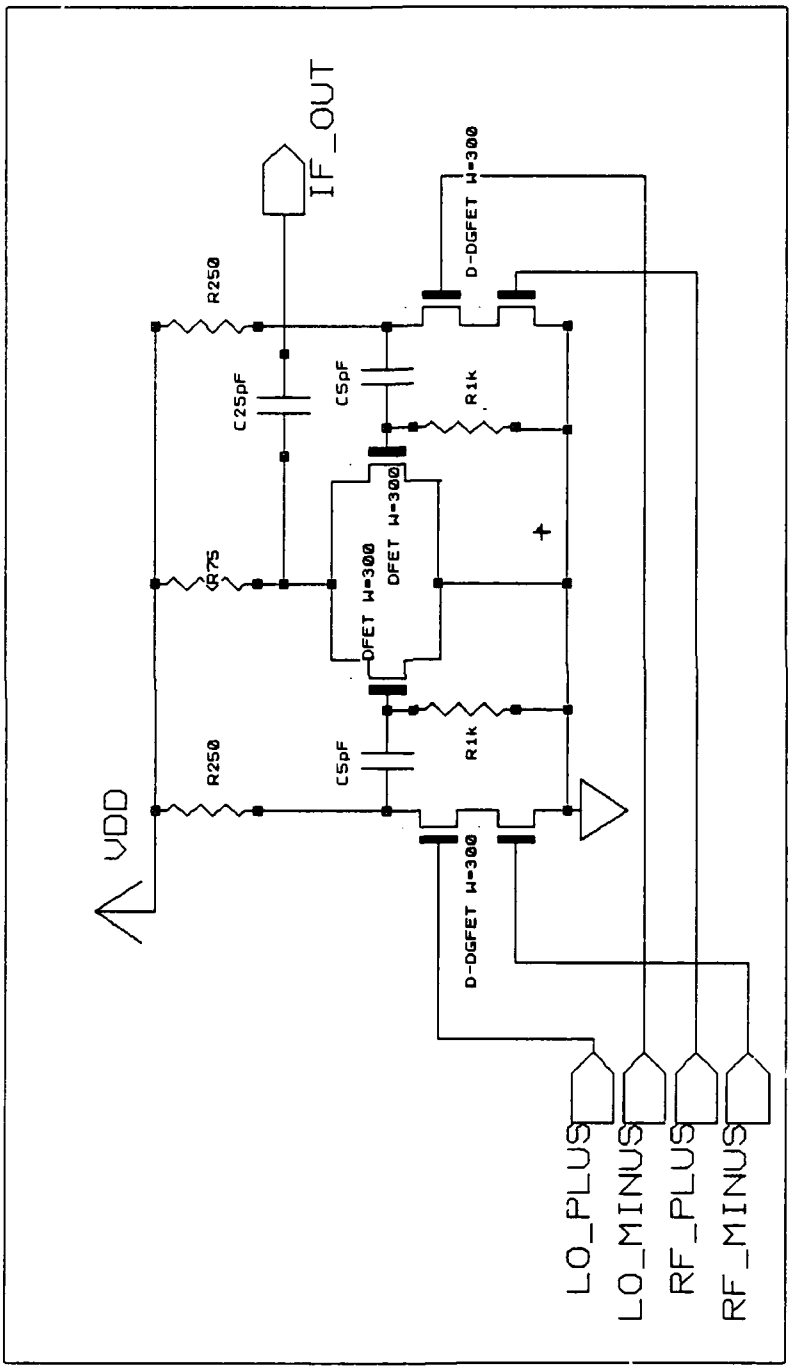

Figure 3.3.2.1.4 Final Mixer Configuration

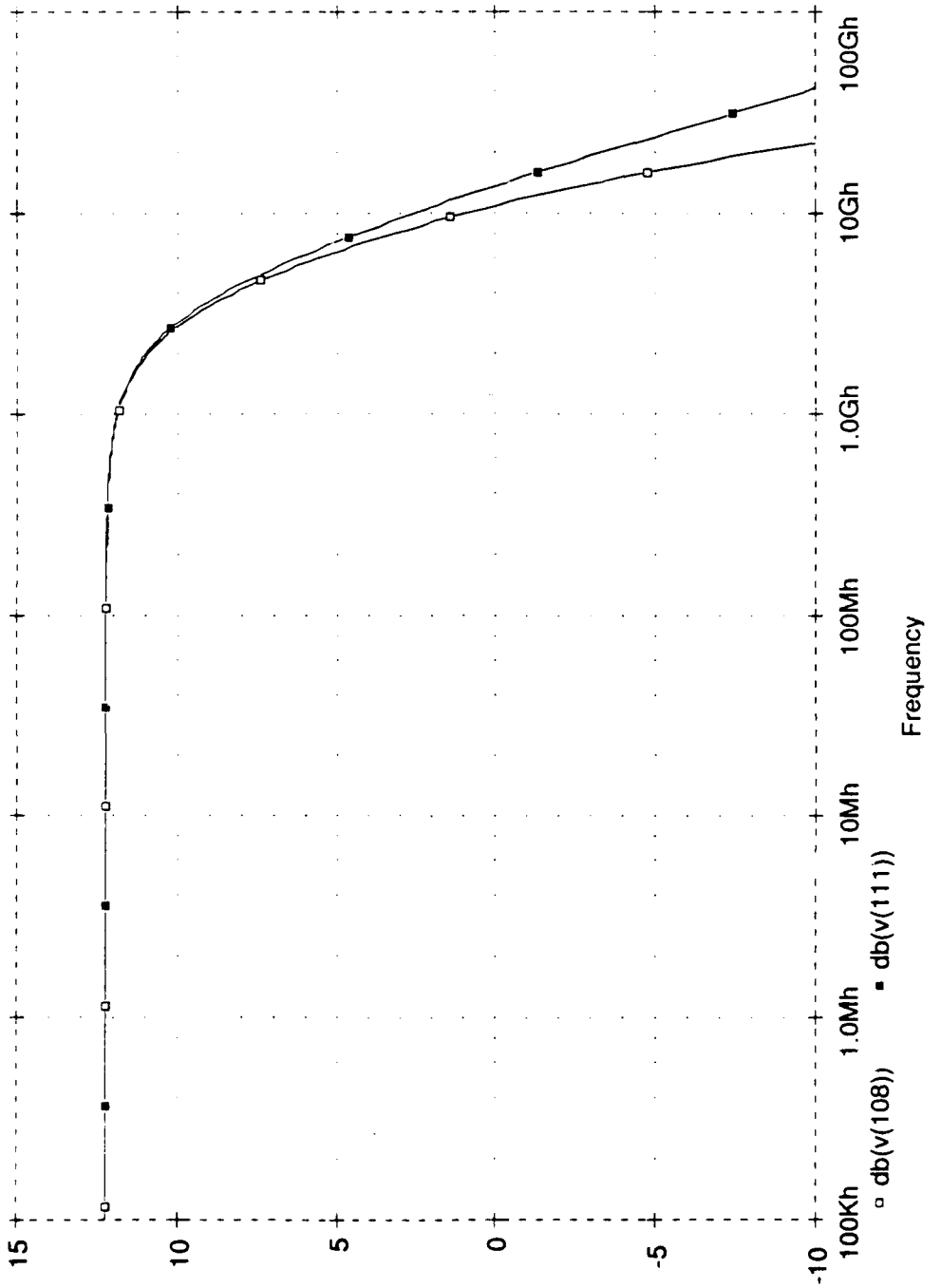

Figure 3.3.2.1.5 Balun Frequency Response.

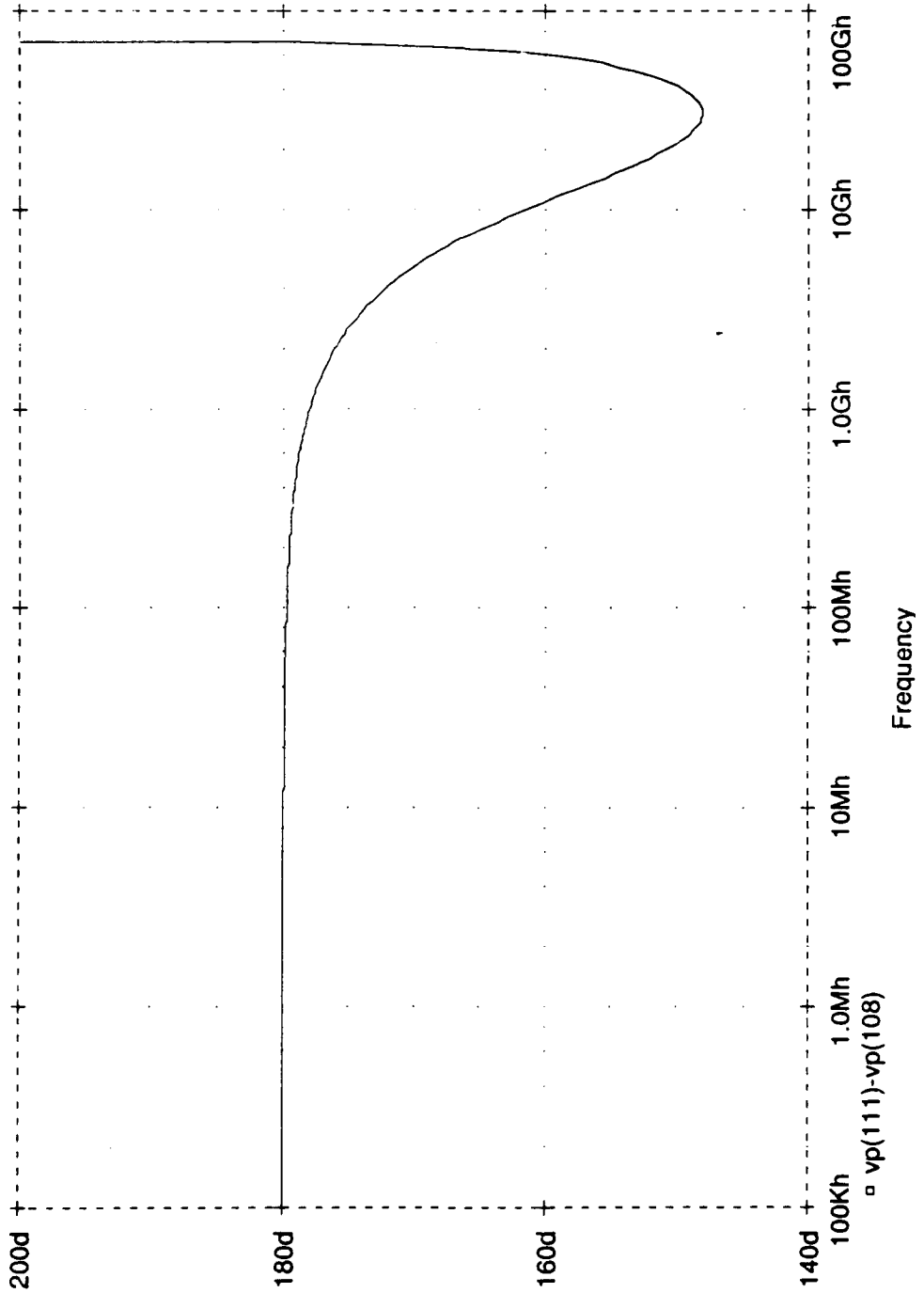

Figure 3.3.2.1.6 Balun Phase Difference at output.

3.3.2.2 Mixer Simulations

Gain

The mixer with baluns shows considerable more gain than the double balance mixer attributed to the gain of the active baluns. Gain as high as 20 dB is achieved (Figure 3.3.2.2.1), however at the expense of additional spurious response that is discussed in the next section. At low RF power levels, the conversion gain is relatively flat an starts to roll off at -16 dBm. (Figure 3.3.2.2.2) Gain versus frequency (for a constant IF) shows greater than 9 dB of gain from .8 to 2.0 GHz. (Figure 3.3.2.2.3)

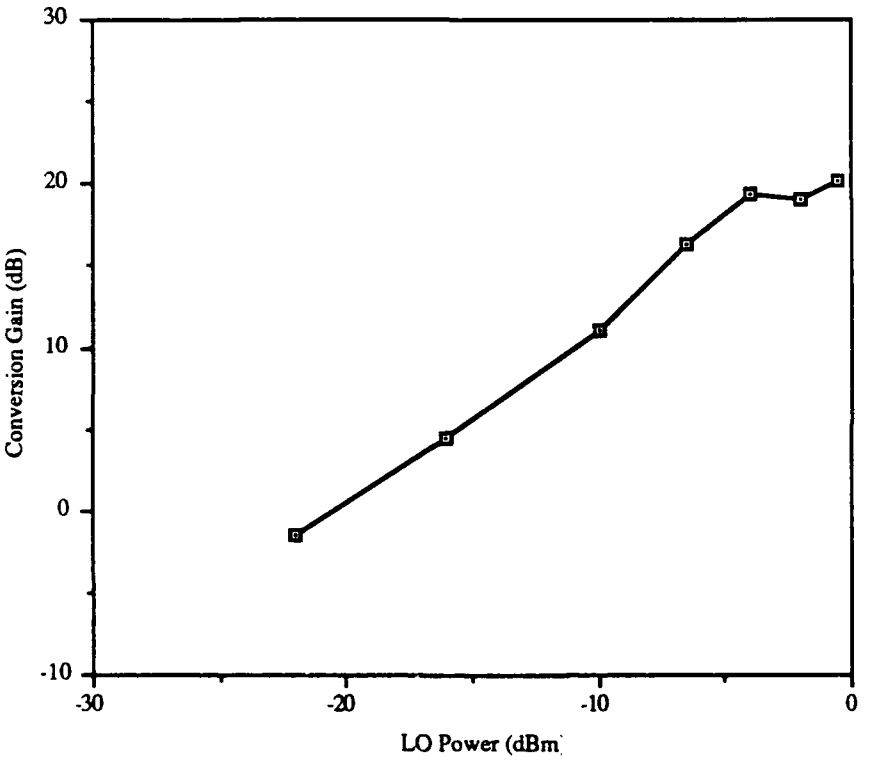

Figure 3.3.2.2.1 Mixer with Baluns Conversion Gain versus LO Power.

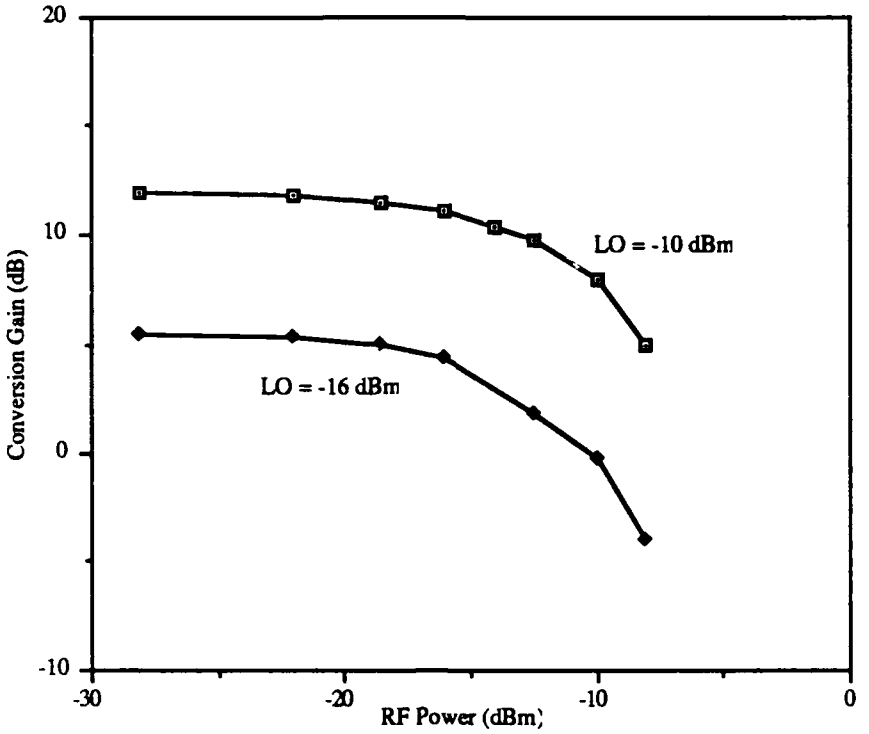

Figure 3.3.2.2.2 Mixer with Baluns Conversion Gain versus RF Power.

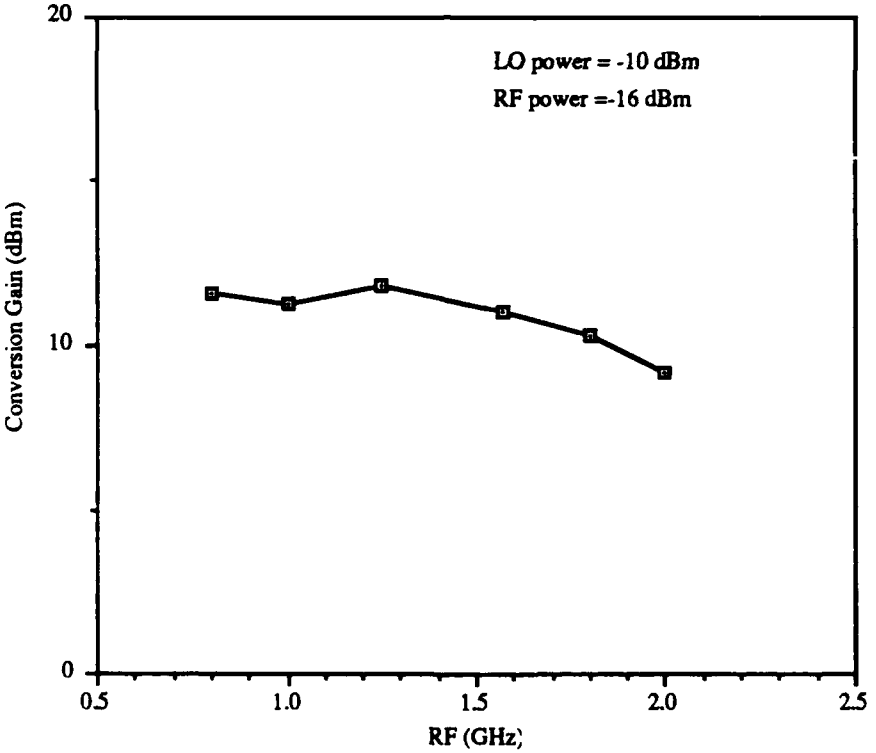

Figure 3.3.2.2.3 Conversion Gain versus frequency.

Intermodulation and Isolation

As mentioned, the overall mixer exhibits a poorer spurious response that the double balanced mixer with ideal baluns. Noteably, there are spurs present that were previously not seen. They are (4,-4), (5,-5), (-2,3), (4,-3), (5,-4), and (-2,4) at .692, .865, 1.056, 2.094, 2.267 and 2.458 GHz respectively. (Table 3.3.2.2.2.1) All of them are easily over 30 dB below the IF especially at low LO power except for (5,-4) at 2.267 GHz and are not a major concern. If the spurs closest to the IF are examined, as seen in Figures 3.3.2.2.2.1 and 3.3.2.2.2.2, the best (2,-2) suppression occurs at low LO powers, whereas the best high order spurs suppression occurs at higher LO powers. The degradation of the LO suppression at the output appears to indicates an imbalance at the input to the mixer. A degradation of 10 dB from an absolute power of -30 dBm would require an amplitude imbalance of 30 mV. As a function of RF power for a median LO power of -10 dBm, (Figures 3.3.2.2.2.3 and 3.3.2.2.2.4) it is not clear that adjusting the RF power will greatly effect the spurious response, but it is encouraging to see over 25 dB of (2,-2) suppression at the lowest RF powers.

The LO/RF port-to-port isolation is exceptional at -45 dB; however, the LO/IF isolation is worse than expected as Figure 3.3.2.2.2.5 indicates. It is important to note the increase in LO isolation as LO power increases implying some LO power affect on phase.

Looking at both the LO and RF power effects on (2,-2) spur, it appears that low power levels provide the best suppression which makes sense when considering the gain of the balun. At the expense of LO suppression, the spurs closest to the IF should be suppressed; therefore, a low power operation is desirable. Figure 3.3.2.2.2.6 is a plot of the spurious response relative to the IF for an RF power of -26.5 dBm and an LO power of -16 dBm. It can be seen that these power settings provide 29 dB of (2,-2) suppression and over 35 dB of suppression of the spurs up to the LO.

Overall Mixer Frequency Products RF = -16 dBm		LO = -22 dBm	LO = -16 dBm	LO = -10 dBm	LO = -6.5 dBm
Product (m,n)	Frequency GHz	Pwr Out (dBm)	Pwr Out (dBm)	Pwr Out (dBm)	Pwr Out (dBm)
(1,-1)	0.173	-17.5	-11.6	-5.0	0.3
(2,-2)	0.346	-43.2	-38.4	-23.0	-21.1
(3,-3)	0.519	-51.4	-46.5	-42.0	-29.9
(4,-4)	0.692	-52.5	-50.0	-46.5	-39.6
(5,-5)	0.865	-52.5	-50.0	-46.5	-39.6
(-2,3)	1.056	-52.5	-50.0	-46.5	-44.0
(-1,2)	1.229	-51.4	-46.5	-34.4	-28.1
(0,1)	1.402	-33.1	-27.4	-22.9	-21.1
(1,0)	1.575	-36.2	-37.3	-46.5	-42.0
(2,-1)	1.748	-56.0	-50.0	-46.5	-42.0
(4,-3)	2.094	-56.0	-50.0	-46.5	-42.0
(5,-4)	2.267	-56.0	-50.0	-46.5	-26.0
(-2,4)	2.458	-56.0	-50.0	-46.5	-42.0
(-1,3)	2.631	-56.0	-42.8	-24.3	-23.2
(0,2)	2.804	-31.7	-19.4	-8.2	-5.2
(1,1)	2.977	-32.3	-25.5	-18.9	-16.3
(2,0)	3.150	-35.2	-33.2	-29.2	-20.5
(3,-1)	3.323	-56.0	-50.0	-50.0	-44.0

Table 3.3.2.2.1 Mixer with Baluns mixing products

Table 3.3.2.2.1 Continued Mixer with Baluns mixing products.

Overall Mixer Frequency Products				
RF = -16 dBm		LO = -4 dBm	LO = -2 dBm	LO = -5 dBm
Product (m,n)	Frequency GHz	Pwr Out (dBm)	Pwr Out (dBm)	Pwr Out (dBm)
(1,-1)	0.173	3.4	3.1	4.2
(2,-2)	0.346	-13.9	-12.7	-11.0
(3,-3)	0.519	-23.2	-23.0	-25.2
(4,-4)	0.692	-32.1	-30.1	-31.1
(5,-5)	0.865	-40.5	-33.7	-32.9
(-2,3)	1.056	-40.5	-33.4	-33.1
(-1,2)	1.229	-23.9	-23.4	-27.1
(0,1)	1.402	-20.3	-17.8	-16.8
(1,0)	1.575	-40.5	-28.6	-21.1
(2,-1)	1.748	-40.5	-36.0	-37.7
(4,-3)	2.094	-32.6	-25.8	-26.1
(5,-4)	2.267	-39.6	-21.4	-21.9
(-2,4)	2.458	-36.2	-33.7	-30.1
(-1,3)	2.631	-20.5	-20.2	-13.5
(0,2)	2.804	-0.4	-0.7	-2.1
(1,1)	2.977	-16.3	-23.8	-21.9
(2,0)	3.150	-16.3	-13.5	-12.1
(3,-1)	3.323	-44.0	-34.7	-29.6

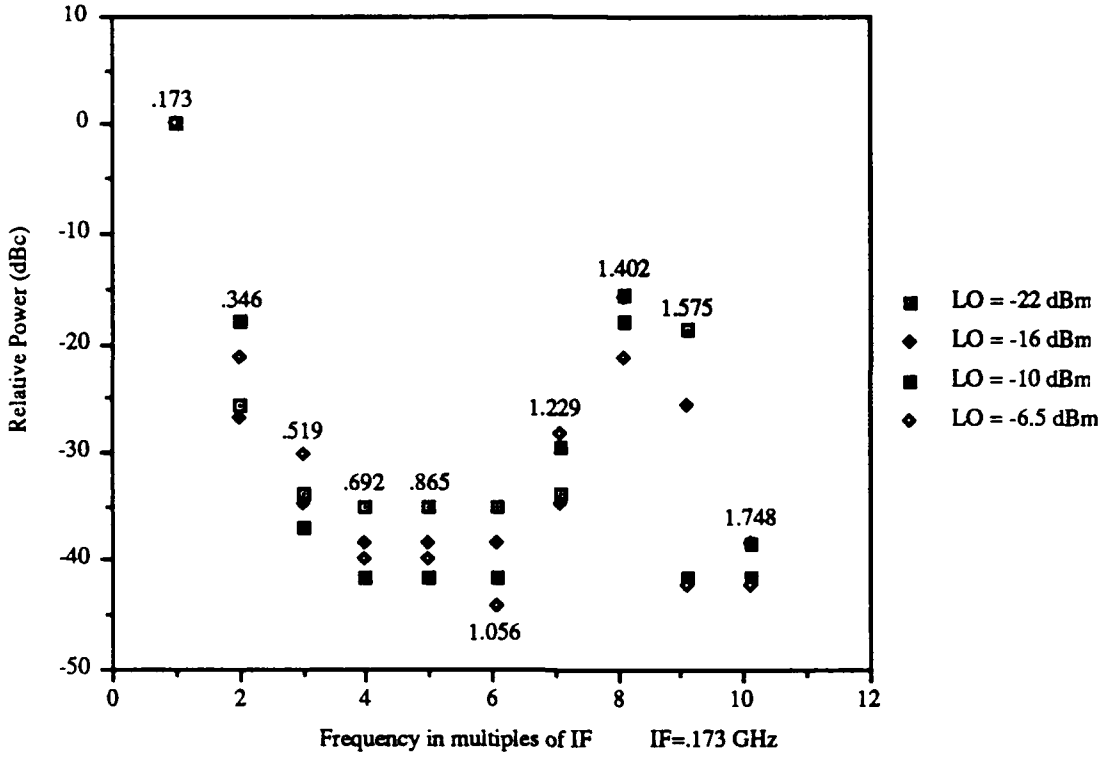

Figure 3.3.2.2.2.1 Output power of spurs relative to IF vs LO power up to 10 IF.

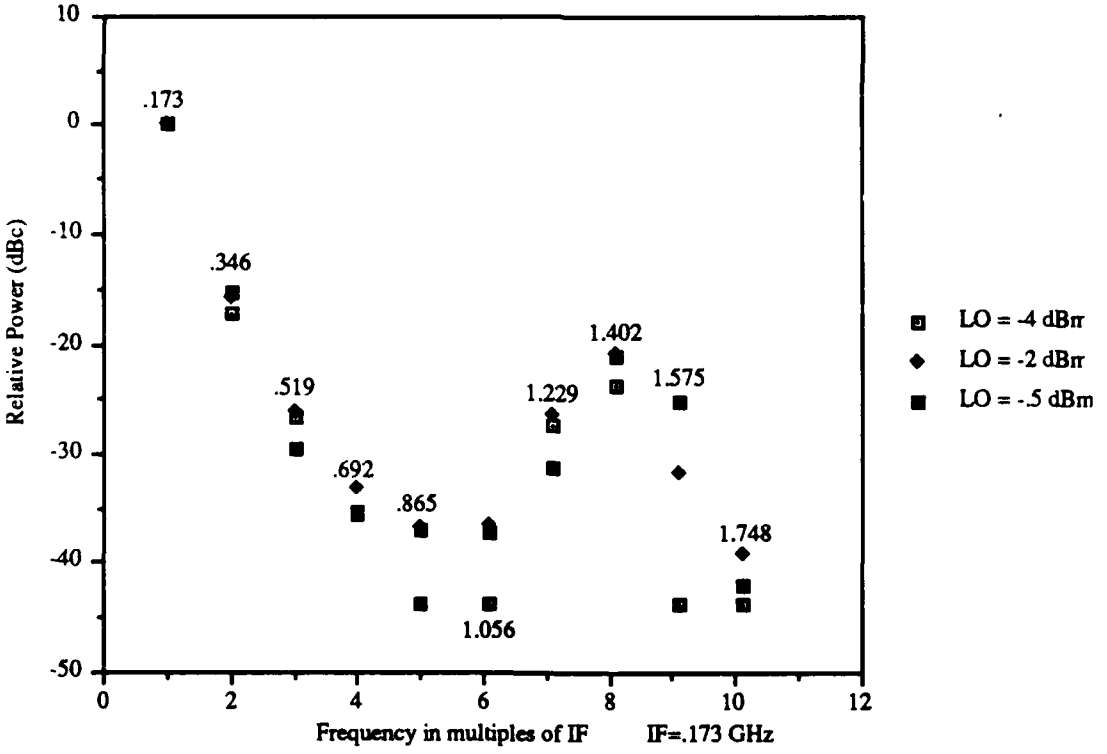

Figure 3.3.2.2.2.2 Output power of spurs relative to IF vs LO power up to 10 IF.

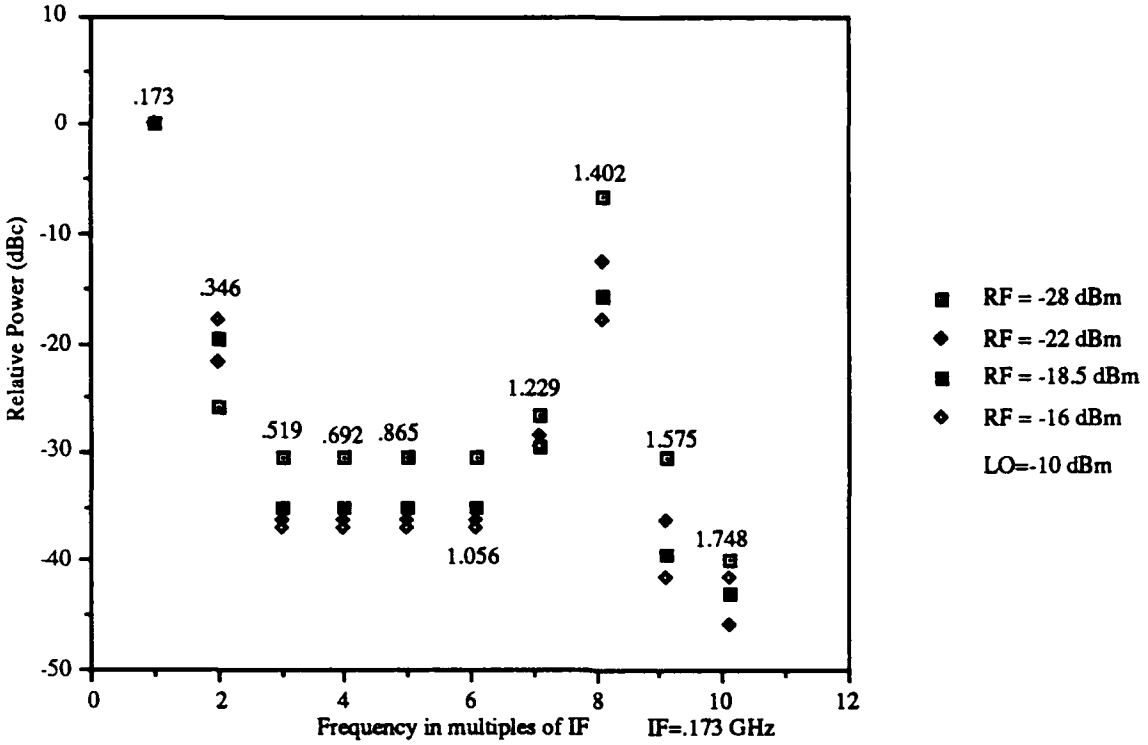

Figure 3.3.2.2.2.3 Output power of spurs relative to IF Power vs RF power

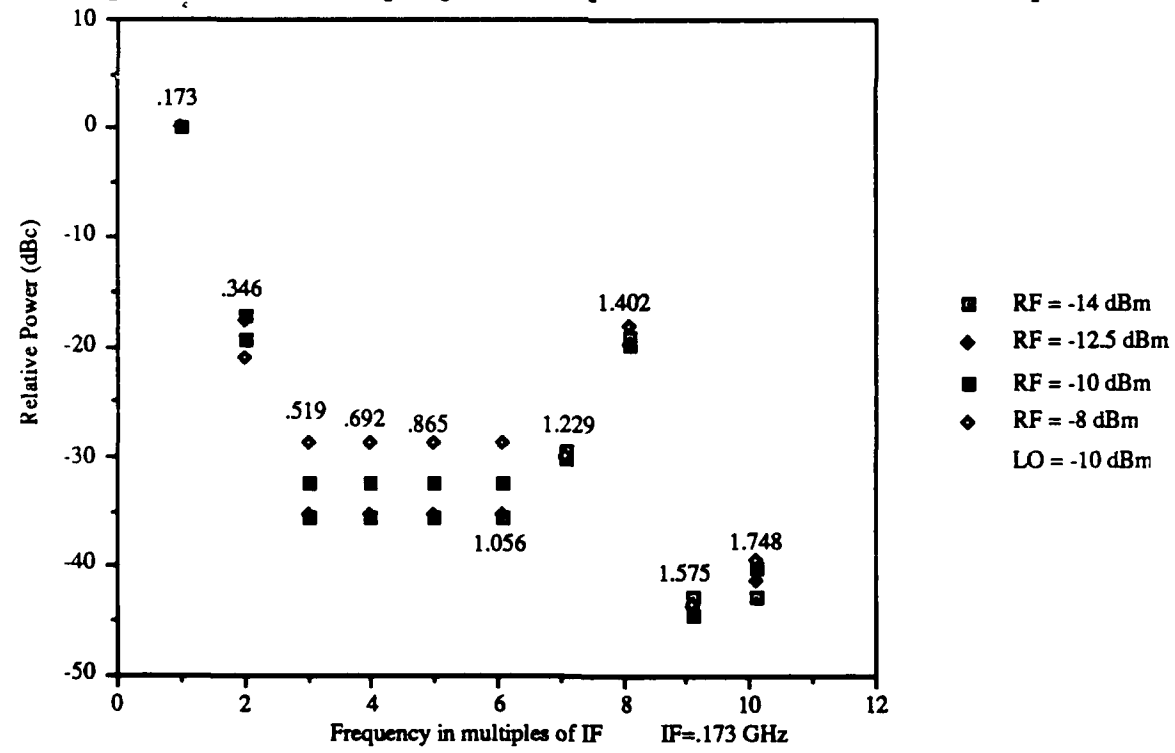

Figure 3.3.2.2.2.4 Output power of spurs relative to IF Power vs RF power.

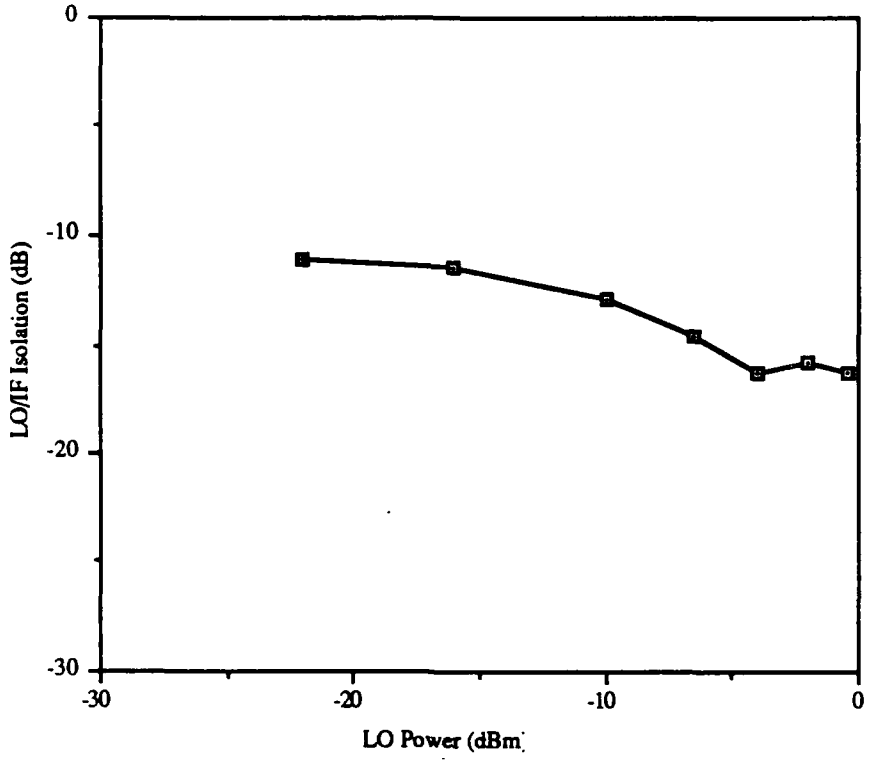

Figure 3.3.2.2.2.5 LO/IF Isolation versus LO power for RF Power =-16 dBm

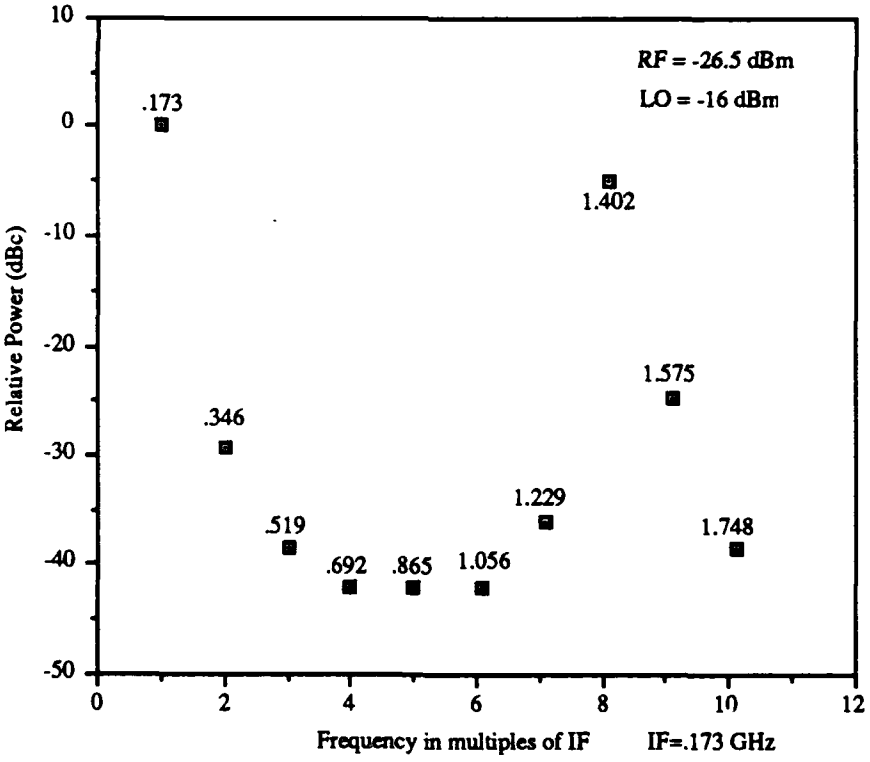

Figure 3.3.2.2.2.6 Output power of spurs relative to IF power for low power operation.

CHAPTER 4

Layout and Fabrication Technology

The objective of this chapter is to describe the layout and fabrication steps used to realize the mixer chip. The QED/A process is briefly described, followed by a description of the layout tool, GDT. The remainder of the chapter presents the actual circuit layouts and examines parasitics.

4.0 QED/A Process

The QED/A process is a GaAs 1 μm enhancement/depletion process offered by TriQuint Semiconductor Inc. of Beaverton, Oregon for fabrication of custom integrated circuits.

In order to appreciate layout constraints, layout parasitics, and how the circuit may be improved, it is very important to understand the types of elements and how they are constructed. In addition to the three types of FETs (E-,D-, and M- as described in Section 3.0), the QED/A process is capable of producing diodes, implanted resistors, precision NiCr resistors, MIM capacitors, and spiral inductors.

4.0.1 FETs

All three types of FETs were are in the mixer circuit, and all are similar in structure except for the channel implants. The basic transistor includes a channel implant overlaid with gate metal, N+ wells and ohmic metal contacts at the source and drain. The difference between the E- and D- type FET is the doping concentration of the channel implant layers, and the M-FET channel is composed of both E- and D- layers. (Figure 4.0.1.1) Typically the FETs exhibit an f_t = 18 GHz and a noise figure of .8 dB at 1 GHz. [22]

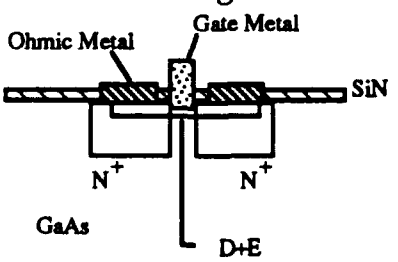

Figure 4.0.1 Typical M-FET.

4.0.2 Diodes

Although the QED/A process is capable of producing a variety of diodes, all diodes used in the mixer were full FET diodes constructed by connecting the source and drain together as shown in Figure 4.0.1.2. Since the FET models are more accurate than the diode models, the full FET diode provided a higher level of confidence in the simulation. However, the current through the full FET diode is limited to 2 mA because of the gate metal current constraints. When necessary, parallel diodes were used to provide the necessary current capability.

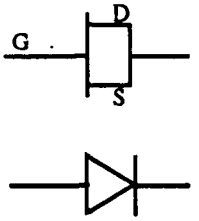

Figure 4.0.2 Full FET diode schematic.

4.0.3 Implant Resistors

The implant resistors are constructed by using enhancement-mode, depletion-mode, or N+ implants (1000Ω, 625Ω, and 125Ω per square respectively) scaled to provide the desired resistance. No implant resistors were used in the mixer circuit because it is difficult to acheive precision with these types of resistors.

4.0.4 NiCr Precision Resistors

NiCr resistors were used exclusively in the mixer circuit. They provide the most accurate resistance and a near-zero temperature coefficient. [15] They are constructed with a thin NiCr strip and a contact on each end. (Figure 4.0.4)

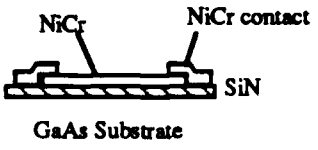

Figure 4.0.4 NiCr precision resistor

4.0.5 MIM Capacitors

The MIM capacitors are simply areas of overlapping interconnect metals with a layer of silicon nitride between the upper and lower plates of the capacitors. MIM capacitors are used in the mixer to provide AC coupling.

4.0.6 Spiral Inductors

Although inductors were not used in the mixer circuit. They will be necessary to improve the mixer performance in the next pass of the design. A spiral inductor consists of a rectangular spiral of airbridge metal.

4.0.7 Interconnect Metal

There are two types of interconnect metal: metal 1 or 1ME and airbridge metal or 2ME. 1ME lays directly on a layer of silicon nitride dielectric except where a dielectric via provides a hole to connect to a circuit element. Airbridge metal, on the other hand, is suspended in the air by dielectric posts. Since it is suspended it may be used to cross over 1ME. Furthermore, since airbridge metal is applied to the wafer after 1ME, it is thicker and provides over twice the current capability. Airbridge metal can only connect to 1ME and must be done with a via through the second layer of dielectric.

Figure 4.1 represents a cut away view of a QED/A wafer taken from Rosario *et al* [15] that pictorially describes how circuit elements are interconnected.

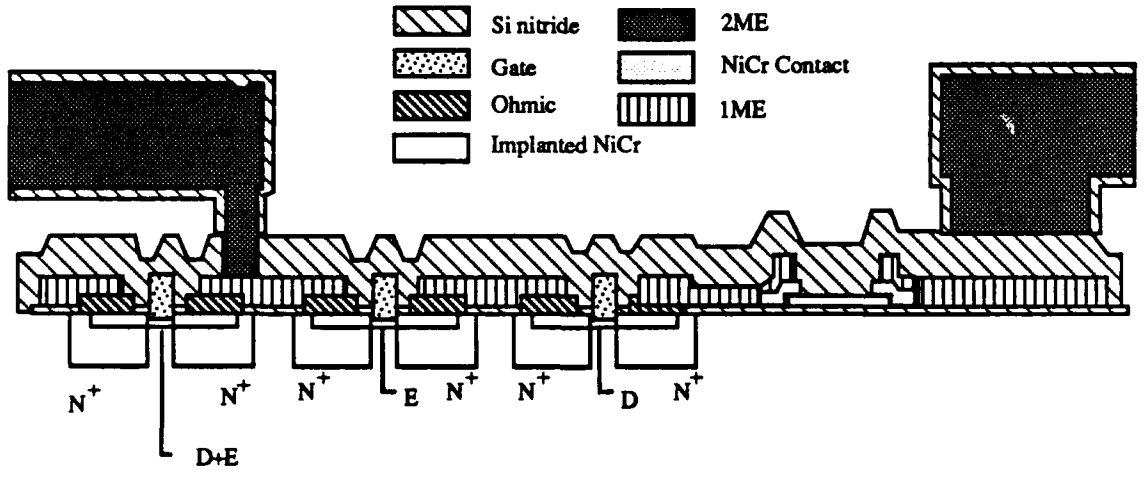

Figure 4.1 Cut away view of typical QED/A wafer.

4.1 GDT Layout Tool

In order to fabricate the wafer, 15 masks were required. TriQuint produced the masks from a CALMA/GDSII file that was generated using Silicon Compiler System's Generator Development Tools (GDT) layout program. A CALMA/GDS II file is simply a set of polygons separated into layers defining a template for each mask Before the mixer could be laid out, the QED/A process had to be incorporated into GDT. This was done by developing a QED/A technology file. GDT looks to the technology file for process layer definitions, transistor geometries, electrical connectivity rules, minimum interlayer and intralayer spacing rules, and interlayer and intralayer capacitances. For example, a depletion mode transistor is defined by a depletion layer rectangle and a gate metal layer rectangle (Figure 4.1.1).

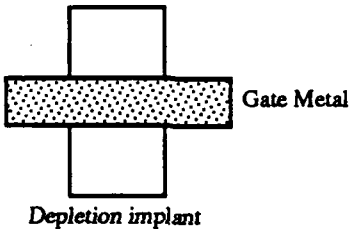

Figure 4.1.1. GDT depletion mode transistor

To complete the transistor as defined in section 4.0, "cuts" must be defined in the technology file. These cuts are used to electrically connect different layers in GDT. The source and drain cuts for a depletion mode transistor include the N+ ion-implantation, depletion, and ohmic metals layers. Therefore, a typical transistor would include the basic transistor and two cuts (Figure 4.1.2).

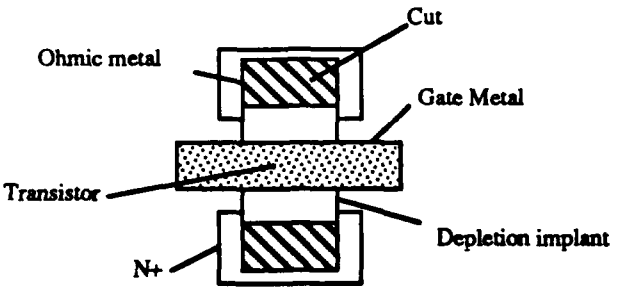

Figure 4.1.2. Typical depletion mode transistor with source and drain cuts added

The source drain cut will allow a metal 1 cut to be added and, therefore, the ability to connect the FET to other circuit elements. When components are connected together using one of the two interconnect metals to form a circuit, GDT is able to generate a SPICE netlist and extract parasitic capacitances between various nodes of the circuit. By simulating from the GDT layout, electrical connectivity is assured. After a layout is complete, GDT uses the spacing rules to determine if any TriQuint design rules are broken.

4.2 Layouts

The circuit schematics from the previous chapter were used to develop the following circuit layouts. Figure 4.2.1 is overall mixer circuit with baluns. Since the resolution is poor the balun section and the double balanced mixer have been enlarged in Figures 4.2.2 and 4.2.3 respectively. Additional circuits were produced (but not presented) in addition to the mixer layout shown: a stand alone balun, a single ended mixer, and duplicate mixer circuits with DC probe pads inserted to measure bias . These ancillary circuits will aide in understanding the operation of the DGFET mixer and help identify the cause of any performance short-comings.

Figure 4.2.2 represents the balun layout with the major components marked. The differential pair is interdigitated to prevent imbalances due to process variations. The remainder of the layout follows the schematic very closely. A DC probe pad is connected to the diode stack (labelled Bias control) that will give some external bias control to amount of current flowing through the current sources. The signal traces leading to the mixer are 3 μm airbridge (labelled output). An additional mixer using 20 μm interconnect

was laid out (Figure 4.2.4) with the intent to measure performance differences between the smallest and largest 2ME traces.

Figure 4.2.3 represents the layout of the double balanced mixer with the major components marked. In order to preserve balance it was important to impose symmetry to the major components of the mixer. Because of the 75 Ω bias resistor at the drain of the buffer FETs, the Touchstone predicts the VSWR at the output to be under 1.6 but with the addition of the AC coupling capacitor the VSWR to degrade to under 2.1 at 173 MHz. Of course, a larger capacitor would improve the VSWR; however, as it is the capacitor is extremely large at 425 μm by 425 μm.

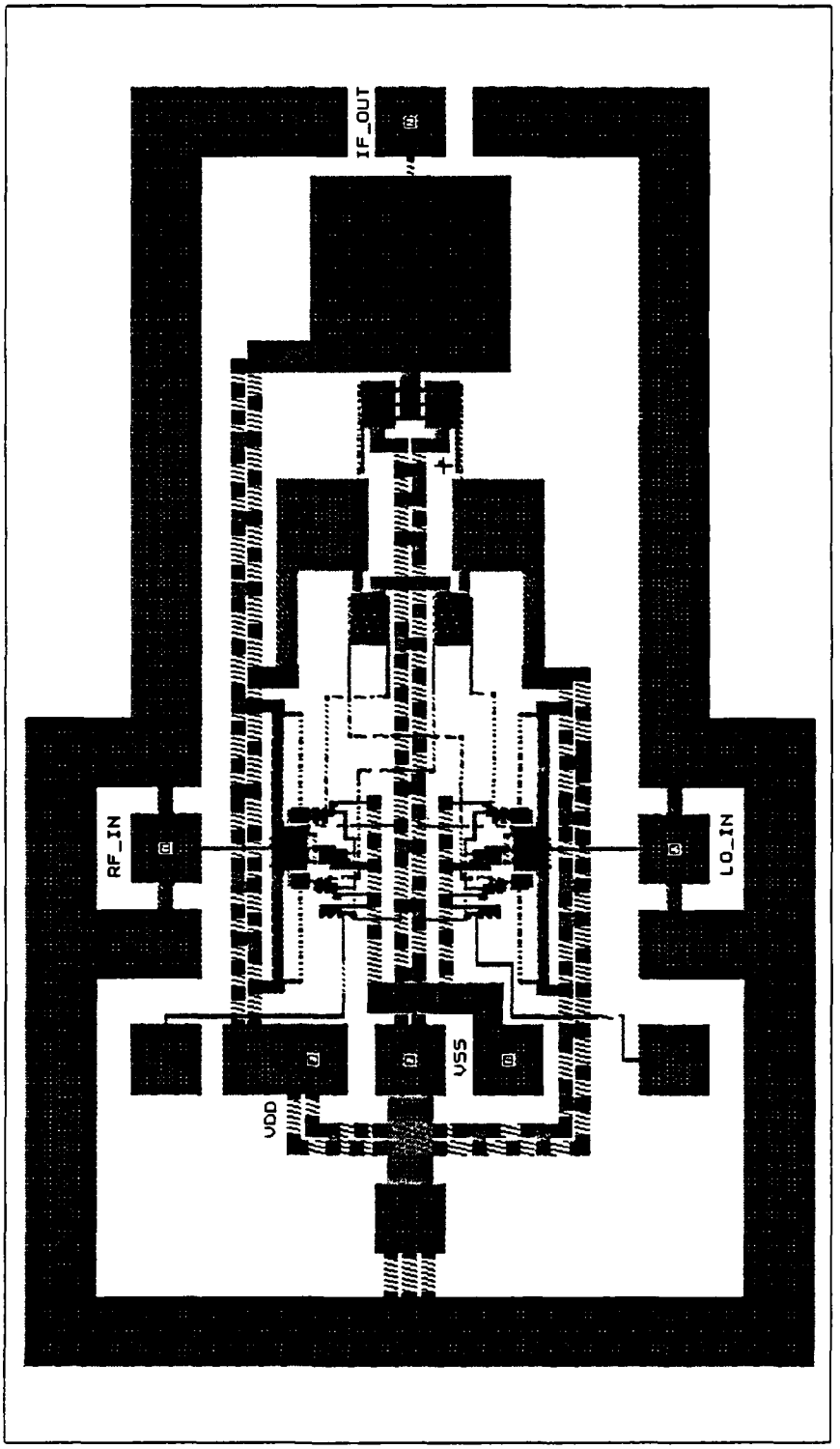

Figure 4.2.1 Layout of mixer with baluns.

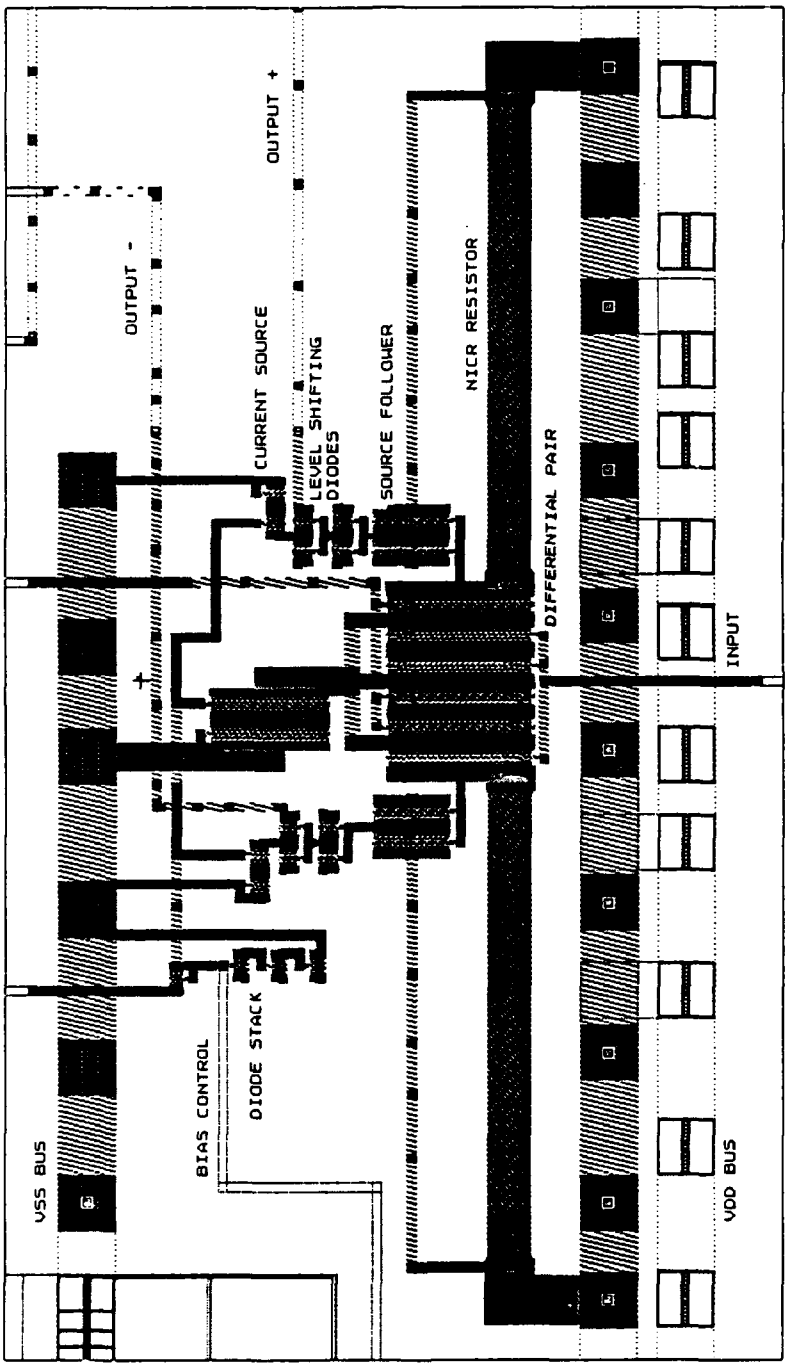

Figure 4.2.2 Balun portion of mixer enlarged.

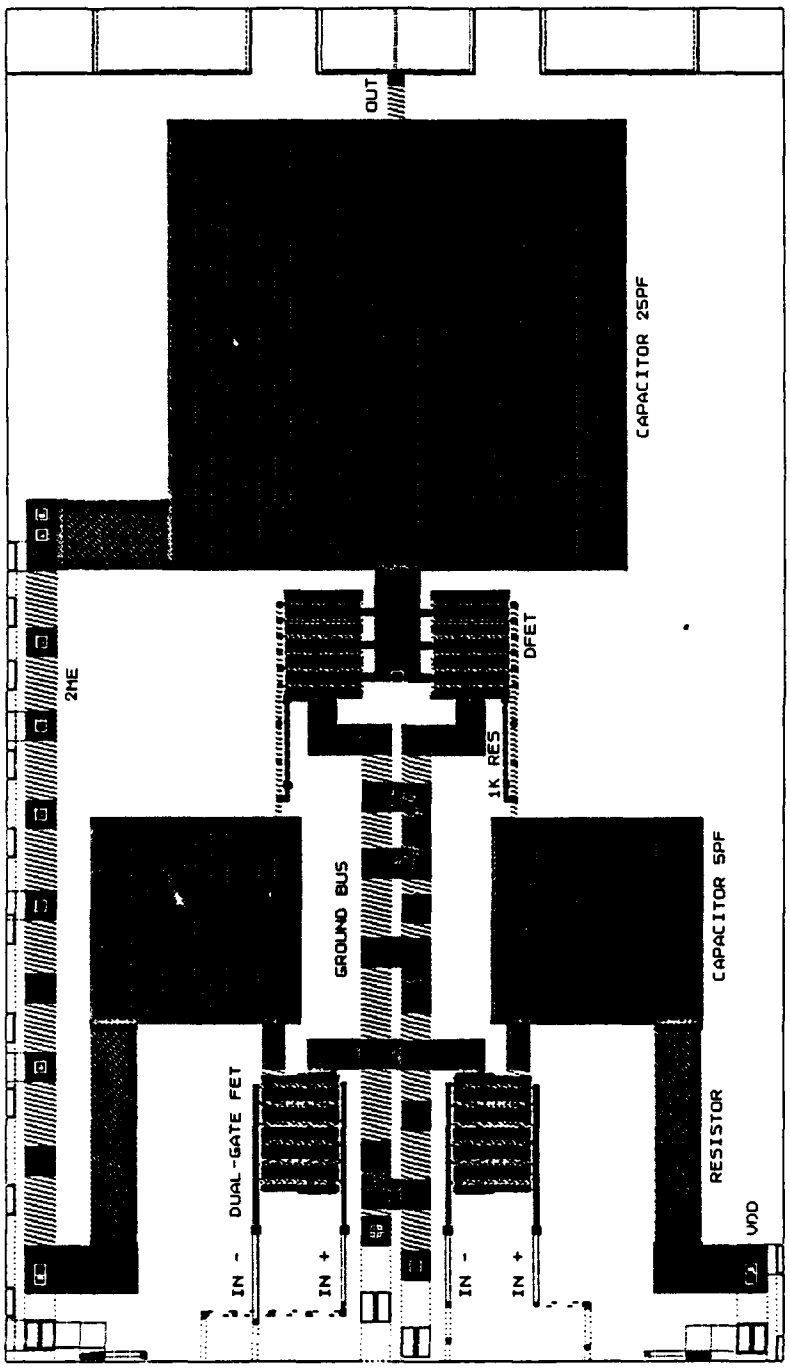

Figure 4.2.3 Double balanced portion of mixer enlarged.

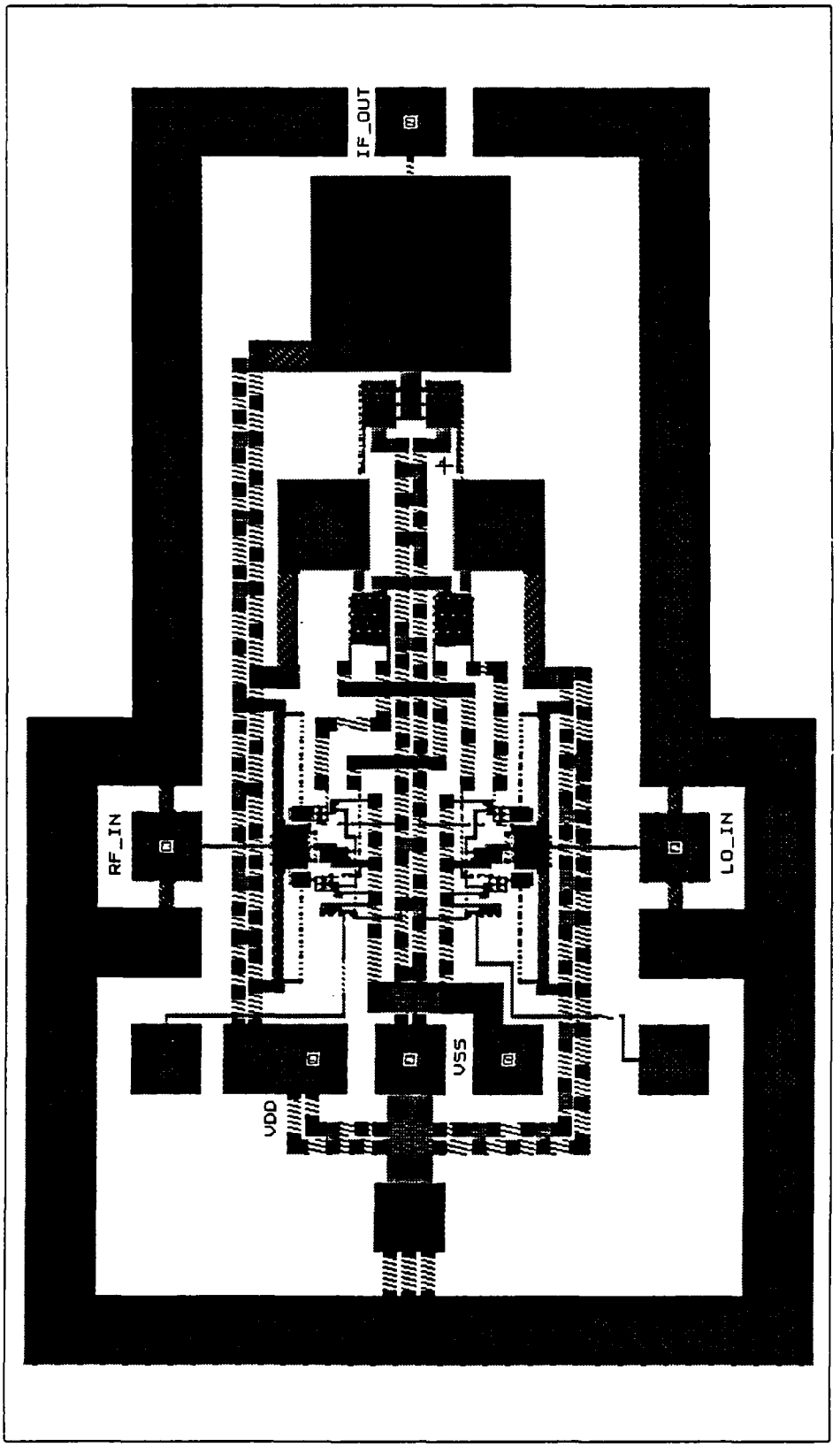

Figure 4.2.4 Overall mixer with balun and wide interconnects.

The mixer was laid out so that the signals (RF_IN, LO_IN and IF_OUT in Figure 4.2.1) could be applied and extracted via 6 mil pitch Ground-Signal-Ground (GSG) probe tips from a Microtech Cascade wafer probe station. Since adequate matching networks were not developed to interface the baluns, two 100 Ω resistors were place in between the signal pads and ground (in parallel) to provide a match to the 50 Ω probe tip. The power is supplied through a Power-Ground-Power (PGP) probe tip. The PGP tip has built in capacitance between the power leads and the ground lead. The +5V supply will be connected to VDD and the -5V supply to VSS. The power was distributed via two 20 μm wide airbridge metal buses capable of handling 100 mA each. Airbridge was selected for its high current capability and ability to cross over 1ME. Two 20 μm wide airbridge metal buses also run down the center of the layout to provide ground. These buses connect to the probe tip ground pads via landed airbridge metal (which is 1ME and airbridge metal laid over each other without the dielectric layers between them). Two additional pads, labelled RFBIAS and LOBIAS, were laid down and connected to the top of the current source diode stack. Since the diode stack controls the drain to source voltage of the current source current generating FET, if necessary external voltages may be applied to each balun separately via DC needles to adjust the current and thus the bias level into the double balanced mixer.

The entire mixer circuit, including the ground ring measures 1.15mm by 1.8mm. As the amount of blank space indicates, the layout is by no means efficient. Laying out a circuit is as much an art as it is a science. The circuit could probably be reduced by at least a third with better layout practices. For example, the capacitors could be shaped to fill spare area instead of squares; serpentine resistors could replace the straight resistors; both the two DGFETs and two buffer FETs could be interdigitated possibly , just to name a few. Furthermore, as a mixer in an integrated receiver the pads and ground ring would no longer be present greatly reducing the size.

Figures 4.2.5 and 4.2.6 represent to two interconnect configurations used to connect the baluns and mixer. The first configuration (Figure 4.2.5) uses the smallest traces possible (3 μm) reducing the paracitic cross over capacitance and coplanar coupling capacitance at the expense of more resistance and inductance. The second configuration (Figure 4.2.6) uses the largest traces possible (20 μm) without going to landed airbridge interconnect reducing resistance and parasitic inductance. The parasitics of these two

configurations will be analyzed to provide an appreciation of layout parasitics and layout tradeoffs.

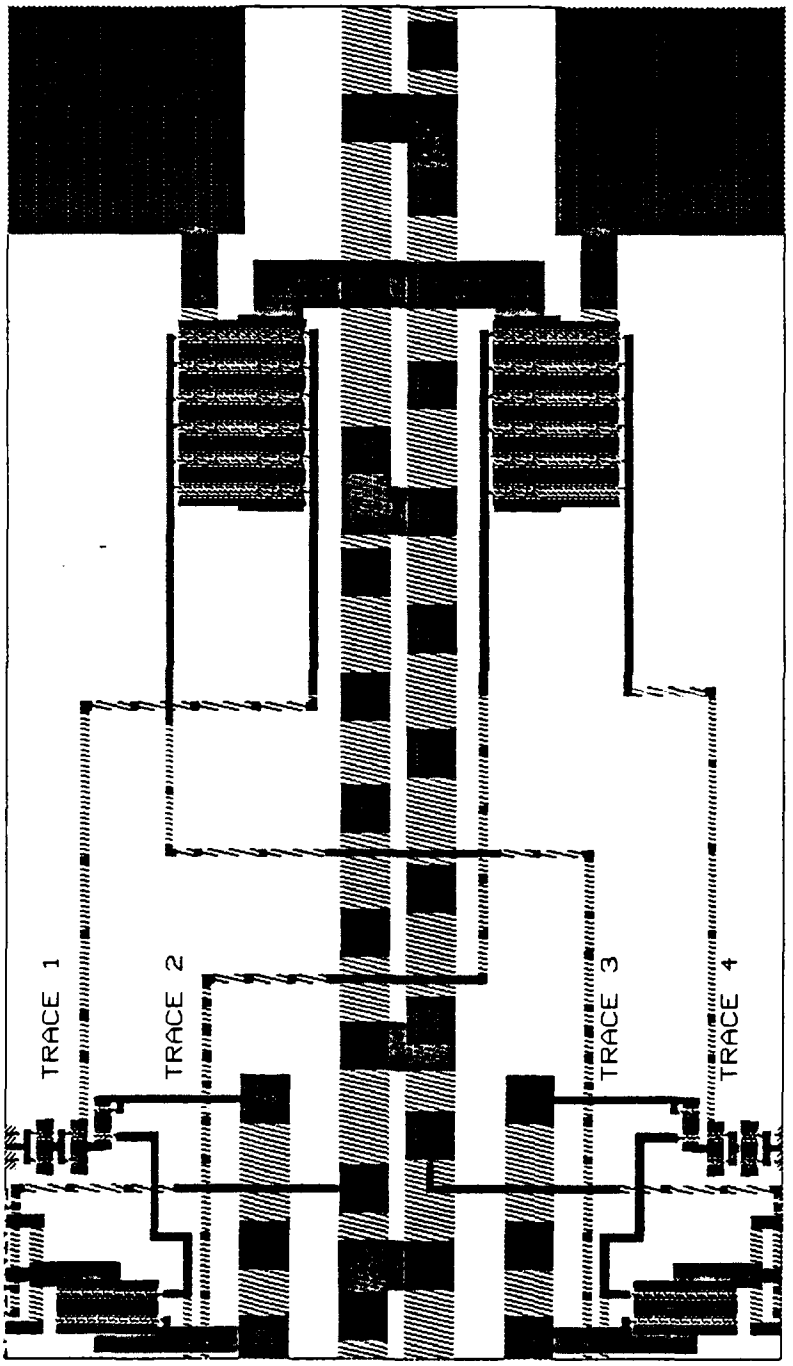

Figure 4.2.5 Enlarged view of 3 μm interconnect.

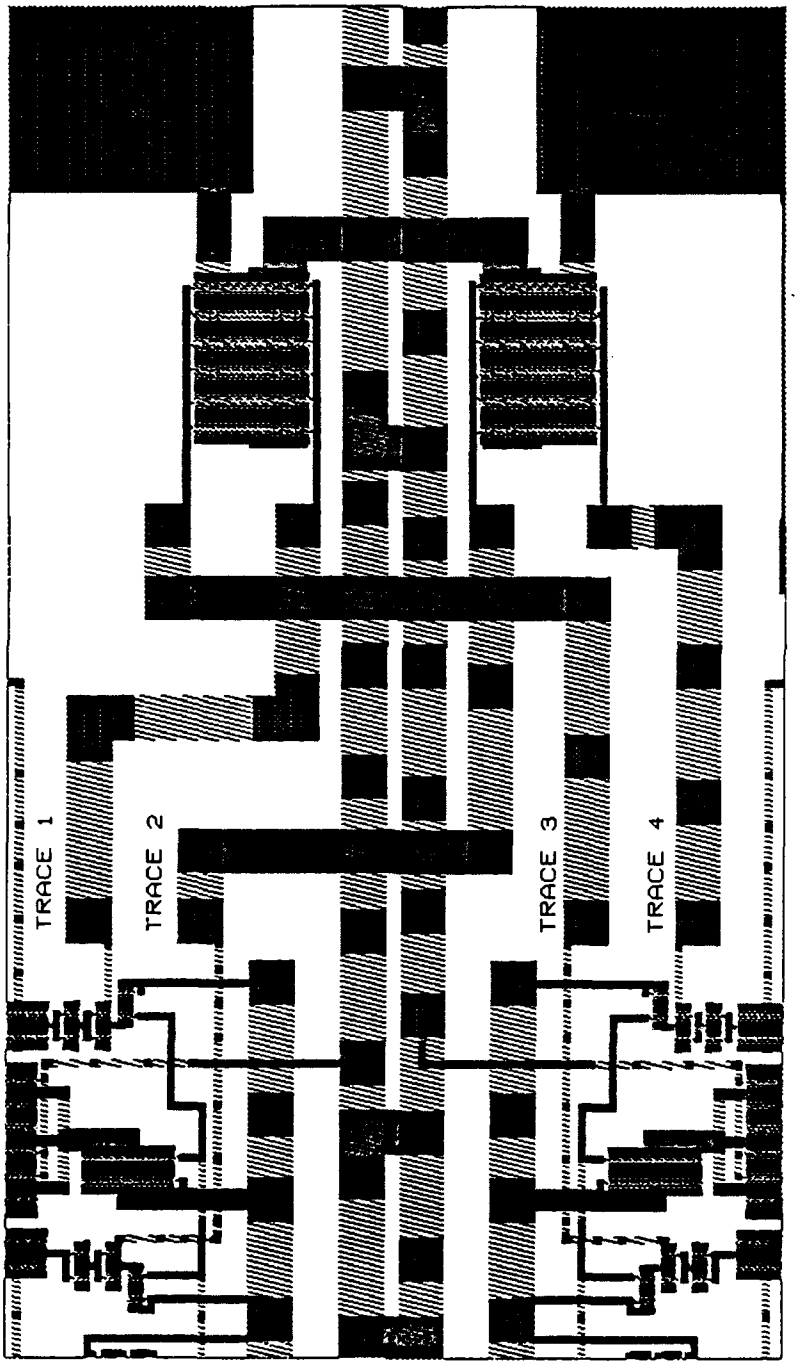

Figure 4.2.6 Enlarged view of 20 μm interconnect.

4.3 Parasitics

There are many characteristics of an integrated circuit that create deviations from an "ideal" circuit. First and easiest is the fact that all interconnect metal has resistance. Even though the sheet resistances of 1ME and 2ME are very low, when compared to the width to length ratio of some interconnect traces, the corresponding resistances can cause problems if not addressed. For example, the worst case sheet resistances for 1ME and 2ME are 30 mΩ/square and 110 mΩ/square respectively. Therefore, for every 3 μm of a 3μm wide 2ME trace would produce 30 mΩ of resistance. Table 4.1 compares the resistances of traces 1 through 4 for both interconnent layouts.

Balun/Mixer Interconnect Resistances (Ω)		
Width	3 μm	20 μm
Trace1	4.50	0.42
Trace 2	6.03	1.00
Trace 3	6.80	1.28
Trace 4	3.73	0.35

Table 4.1 Balun/mixer Interconnect Resistances.

For higher frequencies, the resistances would be higher because of the skin depth, but for 1.575 GHz the lower values hold. The table shows that for even the longest and thinnest traces on the chip the resistances are low. Since the the interconnect traces carry gate currents on the order of μA these resistances are negligible. Except for the power and ground buses which carry large currents, the "parasitic" resistances are ignored. The V_{DD} power bus that wraps around the lower portion of the chip in Figure 4.2.3 is 1400 μm long and could have a resistance as high as 1.05 Ω. PSpice predicts 37 mA through the bus and, thus. a drop of .04 V by the end of the bus which is acceptable.

When it comes to inductive and capacitative parasitics, the fact that the mixer operates at relatively low frequencies means many of the parasitics may be ignored. Of course, in reality, every piece of interconnect on a circuit is coupled with paracitic capacitance and inductance with every other piece of interconnect; however, in practice only certain situations warrant

consideration. In general, especially at low frequencies, the parasitics that are important are the self-inductance of a signal path, crossover and coplanar capacitances between signal paths and crossover and coplanar capacitances between signal paths and ground. GDT is supposed to be able to extract the parasitic capacitances; however, at the time the layout was done GDT was unable to extract the parasitics for the TriQuint QED/A process with any sort of accuracy. Therefore, the capacitance extraction was done by hand.

Since all signal traces are 20 μm or smaller and the substrate is 635 μm thick with no ground plane, when signal traces were long they were modeled as small inductors instead of microstrip lines. The inductance values were calculated from the self-inductance created by treating them as straight retangular (cross-section) bars. Considering the two extreme trace widths, Figure 4.3.1 is a plot self-inductance versus the length of 3μm and 20μm wide 2ME traces.

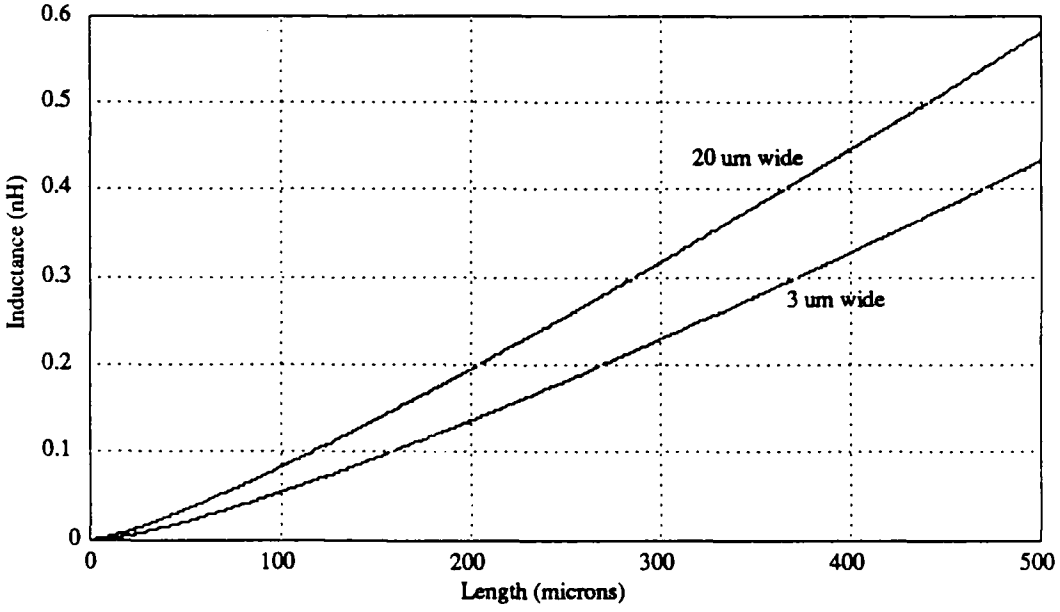

Figure 4.3.1 Self-inductance for 3 μm and 20 μm traces versus length.

The equation used (4.3.1) is taken from a TriQuint Design Manual [] that references work done by Grover [25] and Grupa [26].

$$L = 2l\{\ln[2l/(W+t)]+0.5+.2235[(W+t)/l]\} \qquad (4.3.1)$$

where

L=self-inductance in nH

l=length in cm

w=width in cm

t=thickness in cm

From the physical dimensions of Figures 4.2.6 and 4.2.7, the parasitic inductances are presented in Table 4.2.

Balun/Mixer Interconnect Inductances (nH)		
Width	3 μm	20 μm
Trace1	0.25	0.12
Trace 2	0.21	0.19
Trace 3	0.32	0.25
Trace 4	0.20	0.21

Table 4.2 Balun/mixer Interconnect Inductances.

It can be seen that the large trace width does reduce the self-inductance by a large percentage but not much on an absolute scale.

Since the ground is around the circuit instead of below, there are two types of parasitic capacitances. The first is the capacitance created from 2ME crossing over 1ME. A worst case approximation of the cross over capacitance can be made by calculating the parallel plate capacitance and adding the perimeter distance to the area calculation to take into account the fringe effects. As the area of the overlapping metals increases this approximation approaches the parallel plate value. For a 2ME crossing over 1ME the capacitance can be calculated from

$$C=\frac{A\varepsilon_r\varepsilon_o}{d} \qquad (4.3.2)$$

where A=area, ε_r=1, ε_o=8.854e-12 F/m, and d=1μm. So that the capacitance per area becomes 8.854 mfF/μm^2. The worst case estimates of 3 μm and 20 μm cross over capacitance are .2 fF and 4.3 fF respectively which at 1.575 GHz represent impedances of 500k and 23.5k Ω and can be ignore if it is the only coupling between two given nodes.

The coplanar coupling capacitance per micron between two parallel traces on a dielectric can be calculated from the equations

$$\frac{C}{z} = \frac{1.39e\text{-}17(\varepsilon_r+1)}{\ln(4(1+d/l))} \qquad \text{for } l/d <= .75 \qquad (4.3.2)$$

$$\frac{C}{z} = 2.82e\text{-}18(\varepsilon_r+1)\ln[4(1+2l/d)] \qquad \text{for } l/d > .75 \qquad (4.3.3)$$

where z is the length, ε_r is the relative dielectric constant, d is the separation between the two lines measured from the inside edges, and l is the width of the lines.[28] Figure 4.3.2 is a plot of C/z versus separation, d, for 3 μm and 20 μm lines.

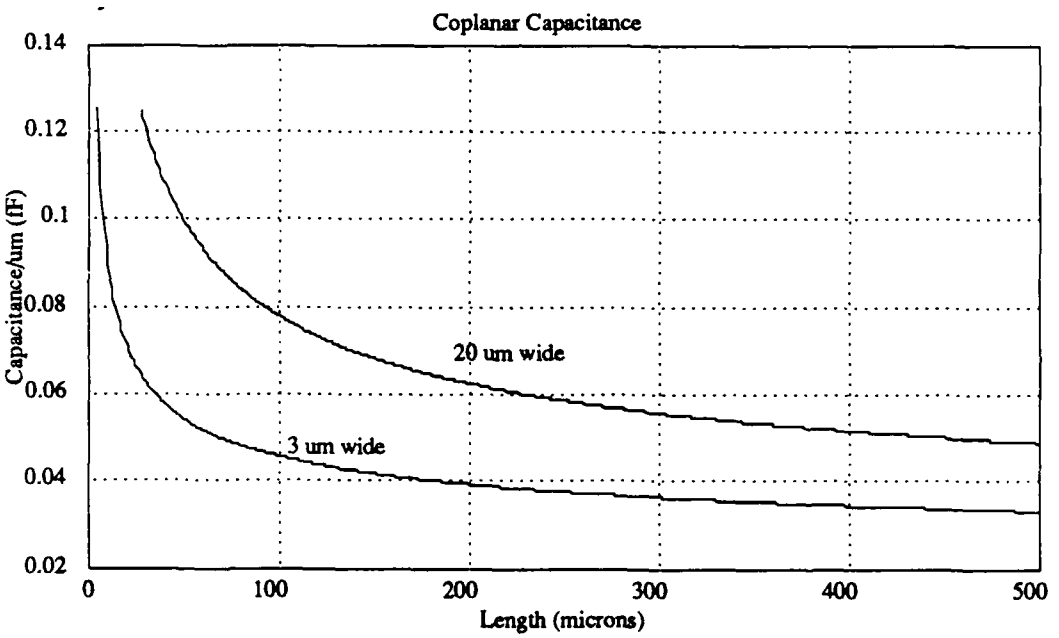

Figure 4.3.2 Coplanar parasitic capacitance for 3 mm an 20 mm traces versus separation for ε_r=12.9.

From these plots, it can be seen that for significant capacitances to occur, the traces must be close together and for a large distance. For example, two 20 mm 1ME traces separated by 30 mm and 150 mm long would have a parasitic capacitance of 15 fF. Furthermore, all of the signal traces, except where necessary, are run in 2ME which has a lower ε_r because of the air dielectric and therefore this plot represents higher capacitances than those of 1ME/2ME and 2ME/2ME interactions. From discussions with TriQuint designers [26]

,they recommend taking the 1ME/1ME value for capacitance and multiplying by 7/15 for 2ME/2ME capacitance and 4/15 for 1ME/2ME capacitance. Therefore, when keeping the capacitative coupling low 2ME and 1ME should be used. Using these calculations, Table 4.3 compares the coplanar parasitic capacitances of the two interconnect schemes. (T_{ij}= capacitance from trace i to trace j)

Balun/Mixer Interconnect Capacitances (fF)		
Width	3 μm	20 μm
T_{12}	4.5	7.6
T_{13}	4.6	6.9
T_{14}	9.8	9.0
T_{23}	5.9	17.5
T_{24}	5.7	6.7
T_{34}	7.5	8.4

Table 4.3 Balun/mixer Interconnect Capacitances.

Figure 4.3.2 reflects the effect of these parasitics on the mixer performance at a LO power of -16 dBm and an RF power of -26.5 dBm. As expected, there is a slight degradation in the LO suppression. However, there is added suppression in the spurs closest to the IF. The gain for the 3 μm interconnect decreased to 2 dB and 1.5 dB for the 20 μm interconnect. Since the layout was constrained by placement of the LO and RF probe tips, for an integrated receiver, these parasitic effects could be reduced greatly by rearranging the baluns to prevent long parallel paths and minimize cross-overs.

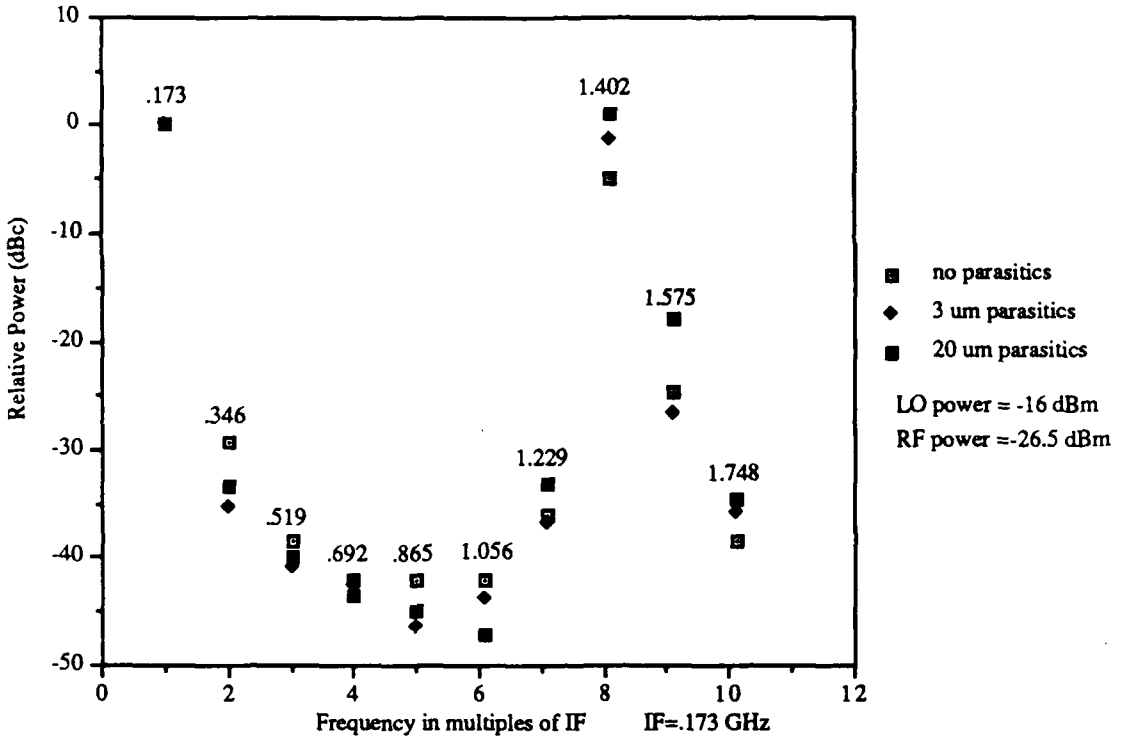

Figure 4.3.2 Parasitic effects on spurious response.

CHAPTER 5

Discussion

The objective of this chapter is to discuss the preferred operating region of the mixer as designed, point out the design deficiencies and recommend changes and new approaches for the next pass of the mixer circuit.

5.0 Preferred Operating Region

Since the bias voltages are set, the preferred operating region becomes a function of signal power. As the simulations indicate, gain is no problem for this mixer. At LO power as low as -20 dBm, unity gain is achieved, and any increase in LO power up to start of balun saturation provides more gain. The LO/RF port-to-port isolation is very good at 45 dB. Therefore, the preferred operating region must be selected on the basis of spurious response and LO/IF isolation. When considering post mixer filtering, the easiest spurs to suppress will be the farthest away from the IF. Furthermore, since the LO/IF isolation is not as good as expected, reaching a maximum of just over 16 dB, selecting power levels that optimize the (2,-2) suppression is the most reasonable approach. As shown in 3.3.2.2.2.6, with the LO power set at -16 dBm and the RF power set to -26.5 dBm, the mixer provides 35 dB of (2,-2) suppression while maintaining gain of 2.0 dB. These operating conditions provide good performance at low signal power. However, with only 10 dB of LO/IF isolation the filtering burden of an integrated receiver has not been greatly reduced. The deviation of LO/IF isolation from the ideal results suggests that there are certain aspects of the design that need to be improved.

5.1 Design Deficiencies and Recommendations

After all is done, the design, the layout, and detailed simulation, there are certain aspects of the circuit that should be refined and incorporated into the next design.

First of all, the balun, as built, exhibits some amplitude and phase imbalance; lowering the load resistance Rd and increasing the differential pair current by a proportional amount should increase the bandwidth without affecting the bias voltage at the input to the mixer. However, this stage has

the biggest effect on gain and must be considered when the adjustments are made. Although, as it will be seen, it is not apparent that this imbalance is a major contributor to the isolation degradation.

Simulations of the single DGFET with the buffer amplifier showed that this topology can be used to perform the sufficient mixing without matching. Once this single ended mixer was designed, the intent was to used a balanced approach to suppress the odd harmonics, thus providing LO/IF isolation and reducing post mixer filtering requirements. The simulations using perfectly balanced inputs showed excellent isolation and suggested that the balanced topology was sound. Therfore, if the balun performed reasonably well, the circuit would be a success. After closely examining the mixer LO/IF isolation degradation, it appears the theory was right, but the implementation was not ideal.

The balanced mixer relys on the phase difference and equal amplitudes to provide the LO short at the output. The problem with the circuit topology as built is that the short is created at the output of the buffer stage and not the mixing device. Clearly, the as built circuit does provide some cancelation, otherwise the LO power would be greater that the IF as with the SE mixer. However, without the short at the output of the DGFET, LO power is leaking back to the DGFET gates. The LO voltages back at the DGFET gates no longer maintain proper phase and amplitude balance, and therefore, add to the LO power at the output and degrade the isolation. The simulations involving the ideal balanced signals using signal generators with 50 Ω source resistances did not exhibit this problem. The 50 Ω load at the input to the double balanced mixer was of sufficiently low resistance to prevent the leakage from creating a problem; however, with the balun connected to the mixer there is sufficient impedance to allow a large enough voltage to re-propagate through the mixer. Since the DGFET is a voltage controlled current device, its the voltage at the gate and not necessarily the power that must be considered. Figure 5.1 represents the recommended change to the existing topology.

This topology change maintains all the attributes of DGFET devices, buffer amplifiers, and a balanced approach. While at the same time, it should provide a better LO short.

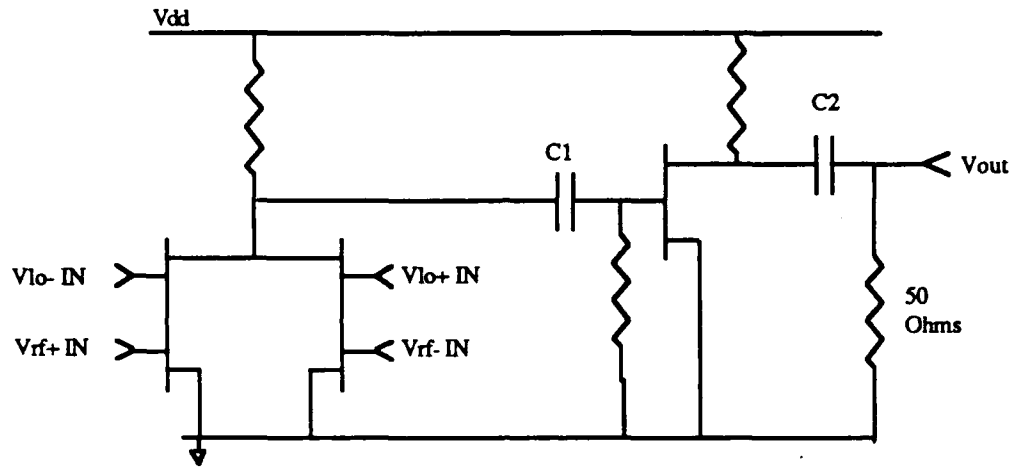

Figure 5.1 Recommended topology change for next design.

5.2 Filtering

The performance of this mixer can be improve with the addition of on chip post-mixing filtering. A low-pass filter with a cut-off frequency as close to the IF as possible, while still passing any modulated signal, would be the desired filter. However, the low frequencies require inductor sizes too large to produce on chip. Since the suppression is good near the IF, the cut-off frequency of the filter may be extended to reduce inductor size, but the order of the filter may have to increase to provide the same suppression. Using a maximally flat low-pass filter with two L/C sections and a cut-off of .7 GHz, reasonable size and LO suppression can be obtained.[21] Figure 5.2 represents the filter stage.

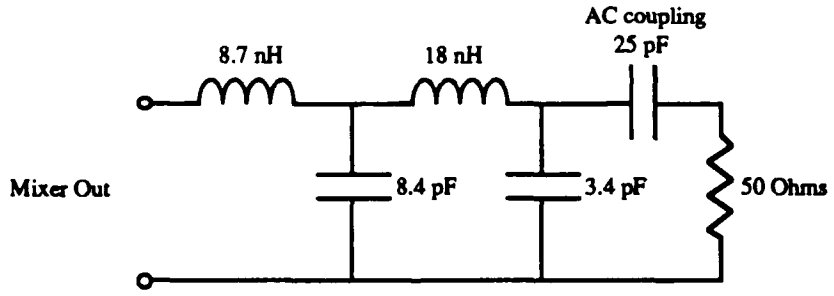

Figure 5.2.1 Maximally Flat Low-Pass Filter with cut-off at .7 GHz.

Simulated results of this filter and the mixer show 33 dB of LO/IF isolation and a spurious response shown in Figure 5.2.2.

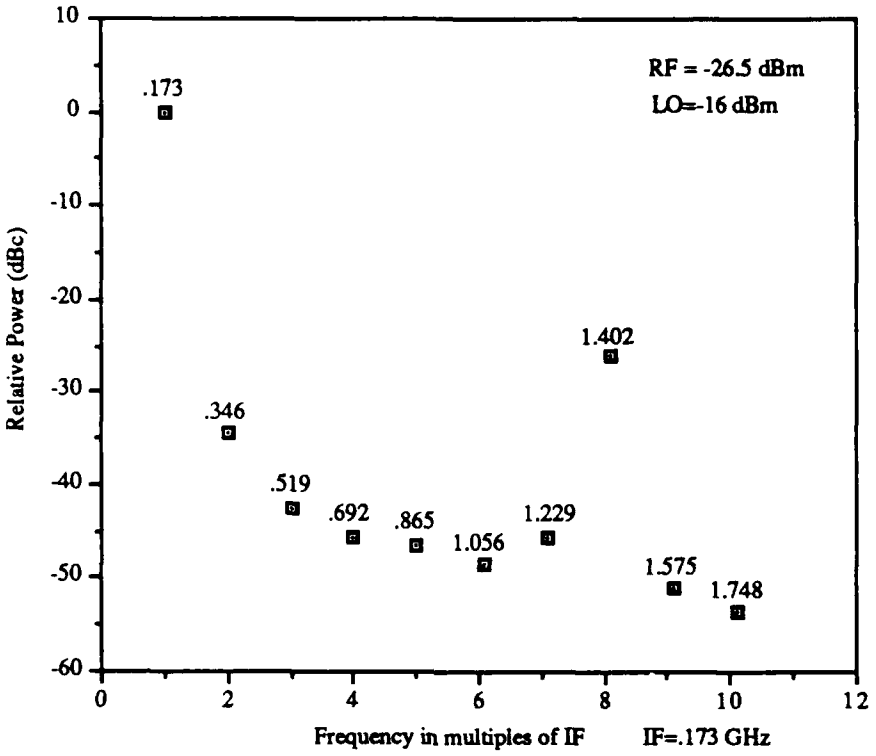

Figure 5.2.2 Output power of spurs relative to the IF with filter.

If the recommended improved topology is used and the LO isolation improved, the cut-off frequency may be extended past .7 GHz; however, a filter will always be necessary to suppress the second order harmonics starting at 2.804 GHz (0,2).

5.3 Testing

The design was included into the first of two planned Draper wafer fabrications at TriQuint Semiconductor. When this wafer returns, the mixer performance will be measured. The measurements will be compared to the simulations contained in this thesis.

CHAPTER 6

Conclusion

This thesis detailed the design, simulation, and layout of a monolithic dual-gate MESFET integrated circuit for L-band mixers using a 1 μm GaAs technology. The circuit utilizes two active baluns and two dual-gate FET mixers to form a single integrated balanced mixer measuring 1.15mm by 1.8mm. The active balun consists of a differential pair to provide the balanced signal and a source follower level shifting topology to bias the dual-gate FET mixers. The level shifting circuits eliminates the need for large AC coupling capacitors and bias networks. The mixing device is a 300 μm depletion mode dual-gate FET followed by a 300 μm depletion mode single-gate FET resistor-capacitor coupled buffer amplifier. The buffer amplifier reduces the size requirements by replacing a matching network at the IF port.

Simulations with PSpice indicate that this circuit can operate at very low LO powers and still provide gain. At an LO power of -16 dBm, the mixer provides 2 dB of gain and good spurious suppression close to the IF with 35 dB at (2,-2) and up to 40 dB of all spurs up to the LO. The LO/RF isolation is good at 45 dB. However, the LO/IF isolation at these powers is not very good at only 10 dB. Both the gain and LO/IF isolation may be increased with the addition of more LO power but at the expense of adding more power to the low frequency spurs. With a small change in circuit topology as discussed in Chapter 5 the LO/IF isolation should be greatly increased at all LO powers.

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